AD-A113 129 MICROWAVE ASSOCIATES INC BURLINGTON MA F/G 13/8
MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR--ETC(U)
JUL 79 Y ANAND DAAB07-76-C-0039
UNCLASSIFIED DELET-TR-76-0039 NL

2 OF 2
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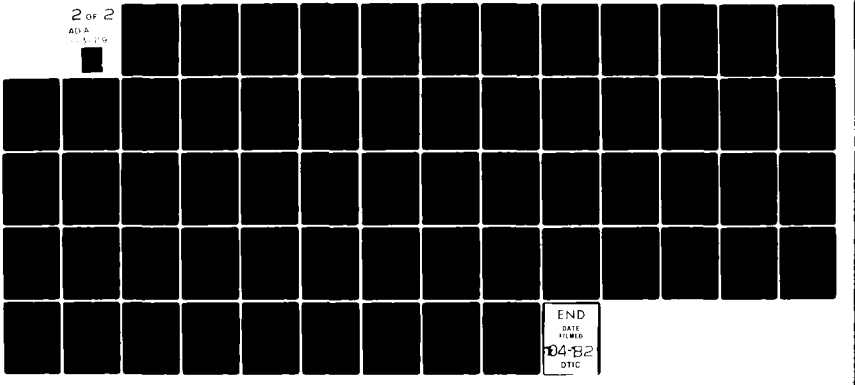

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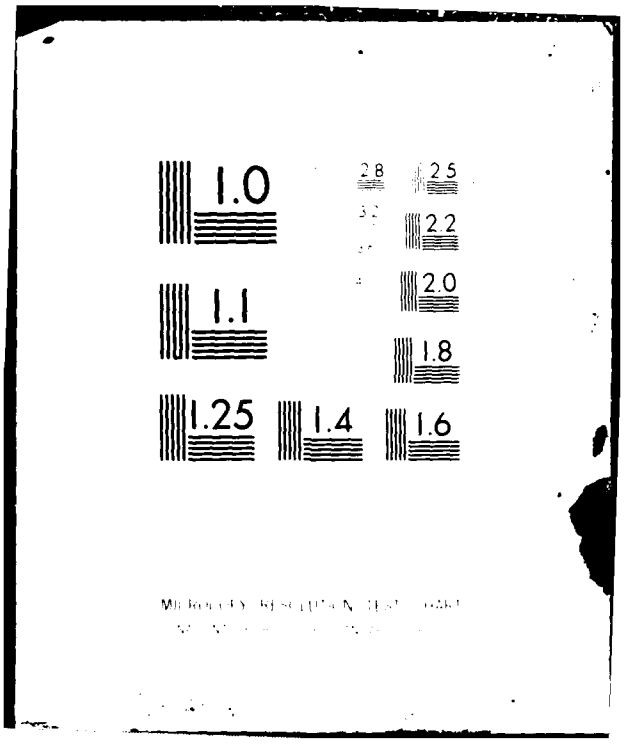
1.0
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PROD. APPROVED	DATE 4/15/78	MICROWAVE ASSOCIATES, INC.	DS - 3940AM	ISSUE
Q. C. APPROVED	DATE 7/17/78	TEST DATA SHEET	SHEET 1	OF 2

SPECIFICATION DRSEL-PP FL108, Revision 1 LOT SIZE 20 SALES ORDER NO.

	INITIAL DATA							AFTER ENVIRONMENTAL TESTS						
PARAMETERS	VSWR	INS LOSS (dB)	FLAT PWR (mW)	SPIKE PWR (W)	RECOVERY TIME 10 dB (μs)	6 dB (μs)	3 dB (μs)	VSWR	INS LOSS (dB)	FLAT PWR (mW)	SPIKE PWR (W)	RECOVERY TIME (μs)	(μs)	(μs)
TEST CONDITIONS	F = 9.0-9.65 F = 9.3 GHz t_p = 0.25 μs P_o = 20 kW DU = 0.001							F = 9.65 F = 9.3 GHz t_p = 0.25 μs P_o = 20 kW DU = 0.001						
MIN. LIMITS								← PERFORMANCE DEGRADATION →						
MAX. LIMITS	1.7	1.3	50	.75	1	2	3	2.0	.3	25	.2	1.0	1.0	1.0
S/N 1	1.28	.7	10	.06	.6	1.2	1.5	1.30	0.1	10	-0-	-0-	0.1	0.2
S/N 2	1.30	.8	45	.16	.7	.7	1.2	1.59	-0-	3	-0-	-0-	0.1	0.1
S/N 3	1.32	.7	6	.04	.6	1.2	1.6	1.56	0.2	14	-0-	-0-	-0-	0.2
S/N 4	1.25	.7	20	.08	.6	1.0	1.6	1.26	0.25	5	-0-	-0-	0.1	0.1
S/N 5	1.31	.7	6	.04	.8	1.0	1.2	1.69	0.25	10	-0-	-0-	-0-	0.1
S/N 6	1.31	.7	2	.04	.7	1.2	1.6	1.50	0.25	0	-0-	-0-	-0-	-0-
S/N 7	1.29	.7	32	.12	.4	.8	1.2	1.30	0.1	3	-0-	-0-	-0-	-0-
S/N 8	1.27	.7	20	.16	.6	1.1	1.6	1.29	0.1	12	-0-	-0-	0.3	-0-
S/N 9	1.31	.7	12	.08	.6	1.0	1.5	1.29	0.1	10	-0-	.1	0.5	-0-
S/N 10	1.30	.7	25	.10	.4	.8	1.2	1.30	.05	7	-0-	-0-	0.15	-0-
S/N 11	1.30	.6	6	.04	1.0	1.6	2.2	1.41	0.2	7	-0-	-0-	0.2	-0-
S/N 12	1.32	.7	32	.12	.6	1.2	1.8	1.46	0.05	3	-0-	-0-	0-	0.2
S/N 13	1.41	.8	25	.15	.6	1.2	1.8	BURNOUT LEVEL: 50 kW						
S/N 14	1.41	.7	20	.09	.7	1.2	1.8							
S/N 15	1.37	1.0	32	.12	.8	1.2	2.0	BURNOUT LEVEL: 21 kW						
S/N 16	1.57	.8	25	.09	.8	1.4	1.7							

TESTED BY [illegible] 7/17/78 Q C APPROVED BY [illegible] DATE 7/20/78

FORM 107 [illegible]

ABLE TO COMMUNICATE

PROD. APPROVED	DATE 4/15/78	MICROWAVE ASSOCIATES, INC.	DS 3940XM	ISSUE
Q. C. APPROVED	DATE 7/17/78	TEST DATA SHEET	SHEET 2	OF 2

SPECIFICATION DRSEL-PP FL108, Revision 1 LOT SIZE 20 SALES ORDER NO.

PARAMETERS	VSWR	INS LOSS (dB)	FLAT PWR (mW)	SPIKE PWR (W)	RECOVERY TIME 10 dB (μs)	RECOVERY TIME 6 dB (μs)	RECOVERY TIME 3 dB (μs)	
TEST CONDITIONS	F = 9.0-9.65	F = 9.3 GHz	P_o = 20 kW	t_p = 0.25 μs	DU = 0.001			
MIN. LIMITS								
MAX. LIMITS	1.7	1.3	50	.75	1	2	3	
S/N 17	1.37	1.1	32	.25	.4	.8	1.2	BURNOUT LEVEL: 31 kW
S/N 18	1.35	.8	20	.10	.6	1.2	1.7	
S/N 19	1.47	.9	32	.12	.5	1.0	1.5	BURNOUT LEVEL: 10 kW
S/N 20	1.50	.8	25	.14	.9	1.5	2.2	
S/N								
S/N								
S/N								
S/N								
S/N								
S/N								
S/N								
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bulk limiters and forty low-level clean-up limiters were assembled and tested to amended specification number P0001, dated 28 April 1978. Forty complete units were shipped to ERADCOM, Fort Monmouth, NJ, upon satisfactory completion of testing. Fourteen units were subjected to various environmental tests. The test results are given in Tables VIII and IX.

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS MA 3940XM	
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 3

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	Li (db)	VSWR		P_f (mW)	P_s (mW)	Rt @3db (μs)	Rt @6db (μs)	Rt@10db (μs)						
TEST CONDITIONS	9.0 - 9.65 GHz			P_o = 20 KW		t_p = 0.25 μs fo = 9.325 GHz		DU = .001						
MIN. LIMITS														
MAX. LIMITS	1.3	1.7		50	750	3.0	2.0	1.0						
S/N 1	.95	1.55		11	50	1.6	<1.2	<0.6						
S/N 2	1.0	1.67		10	14	<1.5	<1.2	<0.6						
S/N 3	1.0	1.56		10	13	<1.5	<1.2	<0.6						
S/N 4	1.1	1.64		8	11	<1.5	<1.2	<0.6						
S/N 5	1.0	1.67		5	10	<1.5	<1.2	<0.6						
S/N 6	1.0	1.56		10	20	<1.5	<1.2	<0.6						
S/N 7	0.9	1.43		10	20	<1.5	<1.2	<0.6						
S/N 8	1.2	1.57		10	20	<1.5	<1.2	<0.6						
S/N 9	1.2	1.57		10	20	<1.5	<1.2	<0.6						
S/N 10	1.0	1.65		10	20	<1.5	<1.2	<0.6						
S/N 11	1.0	1.56		10	20	<1.5	<1.2	<0.6						
S/N 12	1.2	1.68		10	20	<1.5	<1.2	<0.6						
S/N 13	NO UNIT NO. 13													
S/N 14	1.1	1.7			20	<1.5	<1.2	<0.6						
S/N 15	1.1	1.6			20	<1.5	<1.2	<0.6						
S/N 16	1.2	[illegible]				<1.5	<1.2	<0.6						

TESTED BY _____ Q.C. APPROVED BY _____ DATE: 4/12/12

FORM 707 C

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PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS MA 3940XM	
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 3

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	Li (dB)	VSWR		P_f (mW)	P_s (mW)	RT @3 dB (μs)	RT @6db (μs)	RT @10db (μs)
TEST CONDITIONS	9.0 - 9.65 GHz			P_o = 20KW tp - 0.25 μs DU=.001 fo = 9.325 GHz				
MIN. LIMITS								
MAX. LIMITS	1.3	1.7		50	750	3.0	2.0	1.0
17	1.0	1.57		<10	32	<1.5	<1.2	<0.6
S/N 18	NO UNIT NO .	#18						
S/N 19	1.1	1.65		<10	64	2.8	1.9	0.9
S/N 20	1.1	1.61		10	20	2.8	<1.2	<0.6
S/N 21	0.8	1.49		22	100	2.8	1.9	0.8
S/N 22	0.8	1.33		<10	< 20	2.5	1.9	0.5
S/N 23	0.8	1.42		22	44	2.4	2.0	0.8
S/N 24	1.2	1.57		< 10	22	2.0	1.0	0.5
S/N 25	1.3	1.38		< 10	27	1.5	< .5	<0.2
S/N 26	1.2	1.65		< 10	20	1.5	1.0	0.6
S/N 27	1.3	1.55		22	60	< 1.5	<1.0	<0.6
S/N 28	0.9	1.32		< 10	35	2.5	1.8	<0.6
S/N 29	0.9	1.42		< 10	22	2.6	1.8	<0.6
S/N 30	1.1	1.62		< 10	22	2.4	1.8	0.9
S/N 31	0.9	1.33		< 10	30	2.7	1.8	0.9
S/N 32	1.1	1		< 10	40	1.5	0.7	0.5
S/N 33	1.1	1		< 10	45	1.6	1	0.8

TESTED BY. _____ DATE _____ Q. APPROVED BY _____ DATE 4/12/79

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PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS MA3940XM	IS
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 3	OF 3

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	Li (dB)	VSWR		P_f (mW)	P_s (mW)	Rt @3db (μs)	Rt @6db (μs)	Rt @10db (μs)
TEST CONDITIONS	9.0 - 9.65 GHz			Po = 20 kW tp= 0.25 μs DU=.001 fo = 9.325 GHz				
MIN. LIMITS								
MAX. LIMITS	1.3	1.7		50	750	3.0	2.0	1.0
S/N 34	1.1	1.63		10	20	1.5	1.2	0.8
S/N 35	1.1	1.56		10	21	1.9	1.4	0.9
S/N 36	1.1	1.56		10	50	1.5	1.2	0.7
S/N 37	1.0	1.520		10	65	2.9	1.9	0.8
S/N 38	1.0	1.49		10	45	1.7	0.7	0.6
S/N 39	1.1	1.64		10	20	1.5	0.8	0.6
S/N 40	1.2	1.40		10	16	1.4	1.0	0.4
S/N 41	1.1	1.37		12	50	2.7	1.8	0.9
S/N 42	0.9	1.58		18	80	1.7	1.4	0.5
S/N								
S/N								
S/N								
S/N								
S/N								
S/N								
S/N								

TESTED BY _____ Q C APPROVED BY _____ DATE 4/13/xx

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CUSTOMER LEGEND

Customer Army Electronics Com.
Customer P. O. DAAB07-76-C-0039
Part No. Mod P00001
Other Dwg.
*Methods Per

MICROWAVE ASSOCIATES, INC.

LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

PAGE ___ OF ___ PAGES

#	LOT DATE CODE

M/A Type 3940XM
Class
M/A SO No.

	PROGRAM REQUIREMENTS				QTY	REJECTS	NET	Test Limits	Estimated		Actual		REMARKS	Test Oper.
	Examination/Test	*Method No.	Test Conditions						Start Date	Comp. Date	Start Date	Comp. Date		
	Temp. Cycle		-55 to 100°C		3			1 cycle			4/2	4/2	one hour at each temp extreme	JP
	Vibration		.06 inch Double Ampl. 20 to 26 Hz		3			2 planes 20 to 2000Hz			4/3	4/3	15 minutes per sweep	S.S.
88	Shock Non-operating		3 shocks in each plane, 25G		3			6 planes 11 ± 1 mil/sec			4/3	4/3	Total 18 shocks	SC
	Humidity		80% to 98% Relative Humidity -10 to 65°C		3			24 hrs. 1 cycle			4/3	4/4		SC

TABLE IX PILOT LINE SAMPLE RESULTS

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS MA3940XM	
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 2

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS		Li (dB)	VSWR		P_f (mw)	P_s (mw)	R_t @ 3 dB (μ s)	R_t @ 6 dB (μ s)	R_t @ 10 dB (μ s)							
TEST CONDITIONS		9.0 - 9.65 GHz			P_o = 20 kW		t_p = 0.25 μ s			DU = .001						
					f_o = 9.325 GHz											
MIN. LIMITS																
MAX. LIMITS																
		ENVIRONMENTAL TEST RESULTS														
S/N	Post Temperature Test															
S/N																
S/N	36	1.1	1.45		15	40	1.4	1.1	0.8							
S/N	37	1.0	1.57		10	40	2.1	1.6	0.8							
S/N	39	1.2	1.68		< 10	15	1.9	0.9	0.6							
S/N	Post Vibration Test															
S/N	29	1.0	1.48		< 10	10	2.7	2.0	0.7							
S/N	30	1.1	1.61		< 10	< 10	2.1	1.9	1.1							
S/N	41	1.0	1.55		< 10	16	2.2	1.6	1.0							
S/N	Post Shock Test															
S/N	25	1.1	1.5		< 10	12	1.7	< 0.5	< 0.3							
S/N	26	1.1	1.65		< 10	12	1.6	1.1	0.8							
S/N	38	1.1	1.53		< 10	25	1.5	0.9	0.8							
S/N																
S/N																
S/N																

TESTED BY: _____ DATE: _____ Q. C APPROVED BY _____ DATE: 4/12/79

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TABLE IX (cont'd)

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - MA3940XM	
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 2

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	Li (dB)	VSWR	P_f	P_s	Rt @3 dB (μs)	Rt @ 6 dB (μs)	Rt @ 10 dB (μs)
TEST CONDITIONS	9.0 - 9.65 GHz		P_o = 20 kW	f_o = 9.325 GHz	t_p = 0.25 μs		DU = .001
MIN. LIMITS							
MAX. LIMITS							
	POST HUMIDITY TEST						
S/N 19	1.0	1.36	15	50	2.8	2.1	0.6
S/N 31	0.9	1.36	10	60	2.5	1.6	0.6
S/N 34	1.0	1.57	10	15	1.5	1.1	0.6
S/N							
S/N	BURN OUT TEST						
S/N	DU = .001		t_p = 1.0 μs		f_o = 9.325 GHz		
S/N	Burn out level (kW)						
S/N 8	30 kW						
S/N 12	45 kW						
S/N 17	10 kW						
S/N 27	DEG 45 kW	Degraded					
S/N							
S/N							
S/N							
S/N							
S/N							

TESTED BY: _____ DATE _____ APPROVED BY: _____ DATE 4/12/24

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TABI

II. COMPLETE PROCESS SPECIFICATIONS

This section contains the Inspection Plan, Life Test Procedures, Qualification Procedures, and Acceptance Test Procedure.

The Qualification Procedures describe the tests, equipment, conditions and methods of performing qualification approval. The Qualification Procedure is contained in Appendix II .

The Acceptance Test Procedure describes, in detail, the methods and conditions of performing acceptance testing of a limiter. The Acceptance Test Procedure is contained in Appendix III.

III. QUALITY CONTROL ENVIRONMENTAL TEST METHODS

This section contains the Quality Control written especially for this Production Engineering Program. The Manual is contained in Appendix II .

IV. CONCLUSIONS AND RECOMMENDATIONS

On this program, the following achievements were made:

(1) High Power, X-Band, Complete Solid State Receiver Protectors were fabricated in Production quantities.

(2) A low cost, narrow-band unit was also developed for marine radar applications.

(3) Fabrication and delivery of fifteen (15) Engineering Samples; twenty (20) Preproduction Limiters, and forty (40) Pilot Line Limiter Assemblies. Complete life and environmental tests have been conducted on the preproduction and pilot run limiter assemblies.

(4) This work should be pursued at millimeter frequencies, especially at Ka-Band frequencies.

V. PUBLICATIONS

(1) G. Morris, V. Higgins, G. Hall, Y. Anand, R. Billota, and F. Jellison, "Self-Activated, 20 kW, X-Band Bulk Effect Semiconductor Limiter", 1978 GOMAC Conference

(2) G. Morris, V. Higgins, G. Hall, Y. Anand, R. Billota, and F. Jellison, "X-Band, High Power Solid State Receiver Protector Employing a Bulk Semiconductor Limiter", 1979 IEEE, MTT-S-INTERNATIONAL, Orlando, Florida

VI. IDENTIFICATION OF TECHNICAL PERSONNEL

The following key technical personnel contributed to this program:

Y. Anand - Project Manager

P. Schaffer - Silicon Manager

W. Sobie - Metallization Manager

G. Allendorf - Material Scientist

R. Billota - Limiter Manager

S. Ellis - Engineer

REFERENCES

1. K.E. Mortenson and J.F. White, "Non-Refrigerated, Bulk Semiconductor, Microwave Limiters", IEEE Journal of Solid State Circuits, SC-3, pp. 5-11, 1968.

2. K.E. Mortenson et al, "Microwave Solid State Limiting Phenomena", Final Report for AFAL, Contract No. F33615-67-C-1858, November 1968.

3. K.E. Mortenson et al, "A Review of Bulk Semiconductor Microwave Control Components", IEEE Proc., Vol. 59, No. 8 , pp 1191-1200, August 1971.

4. K.E. Mortenson et al, "Bulk Semiconductor Limiters", Final Report for U.S. Army ECOM, Technical Report ECOM-0186-F, August 1973.

5. A.L. Armstrong et al, "Bulk Semiconductor Limiters" Final Report for U.S. Army ECOM, Technical Report ECOM-01950F, October 1971.

6. A.L. Armstrong et al , "Bulk Semiconductor Limiters", Semiannual Report for Contract DAAB07-72-C-0292, March 1973.

7. A.L. Armstrong et al, "Bulk Semiconducror Limiters", Final Report for Contract DAAB07-72-C-0292, March 1974.

8. Y. Anand et al, "MM&T Program For the Etsablishment of Production Techniques for High-Power Bulk Semiconductor Limiters", First Quaterly Report for Contract DAAB07-76-C-0039, ECOM, U.S. Army Electronics Research and Development Command, Fort Monmouth, NJ , October 1976.

9. Y. Anand et al,"MM&T Program for the Establishment of Production Techniques for High-Power Bulk Semiconductor Limiters", Third Quarterly Report for Contract DAAB07-76-C-0039, ECOM U.S. Army Electronics Research and Development Command, Fort Monmouth, NJ., April 1976.

10. Y. Anand et al "MM&T Program for the Establishment of Production Techniques for High-Power Bulk Semiconductor Limiters", Sixth Quarterly Report for Contract DAAB07-76-0039, ECOM, U.S. Army Electronics Research and Development Command, Fort Monmouth, NJ., January 1978.

11. J.F. White , Semiconductor Control, 1977.

APPENDIX I (a)

ORIGINAL SPECIFICATIONS (SCS-486)

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts
MIL-STD-1311A	Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-408/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1 μsec pulses continuous	:	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss	:	0.7dB (max)
(c)	Low Level VSWR	:	1.4:1 (max)
(d)	Recovery Time	:	0.8 μsec (max)
(e)	Flat Leakage	:	50 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(f)	Spike Leakage	:	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias	:	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 [illegible] facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection [illegible] inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance [illegible] zero (0). For purposes of inspection, the lot size shall be one (1) month's [illegible]

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures [illegible]

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance Inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

4.6 Test Conditions

Parameter Unit	T_A °C	Fo GHZ	Po Watts	μ sec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 - 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μsec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformance Inspection - Part 1 (QC 1-1)

	Mil Standard	Application Method	Test Condition	Symbol	Lower	Upper	Unit	No.
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Lower	Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	γ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC III-3)

ES:

e maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4-52 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

A swept frequency may be used.

Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a db increase of limiter insertion loss mpared to the "cold" insertion loss.

Quality conformance test to be made using bulk semiconductor stage only.

For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

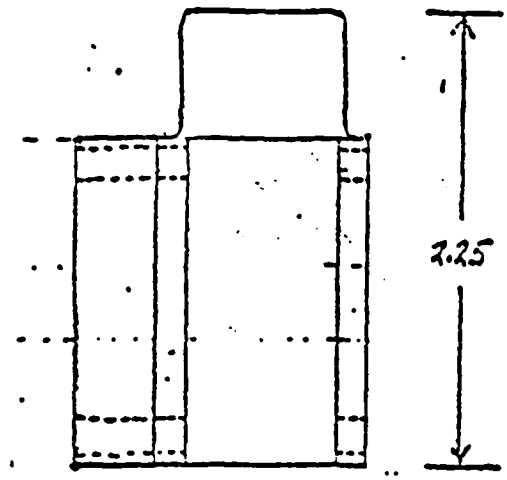
Measurement of parameters cited will follow the procedures outlined in QCI -1.

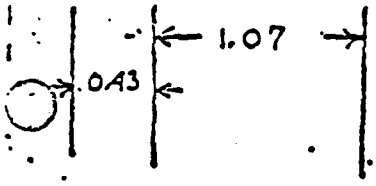
The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s), will be periodically monitored. Life test will be interrupted each 720 ± 20 hours intervals to permit testing of end of life test end points.

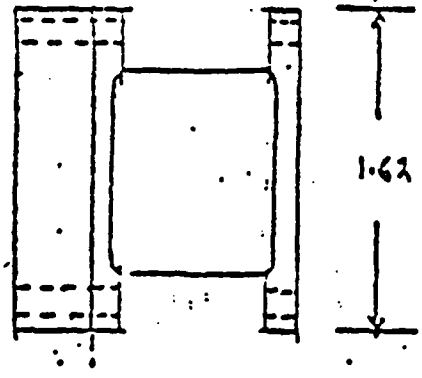
5. PREPARATION FOR DELIVERY

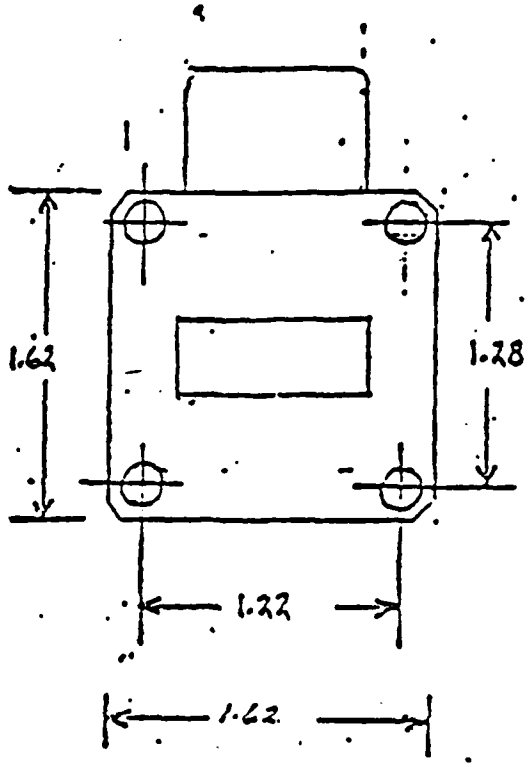
5.1 Packaging, Packing and Marking. - Packaging, packing and package marking shall be specified in the contract.

LINE DRAWING









Notes:

a) all dimensions in inches
b) all tolerances ± 0.01 unless otherwise specified

APPENDIX I (b)

SPECIFICATION (Modification No. P00001)

Modification No. P00001
Supplemental Agreement to
Contract No. DAAB07-76-C-0039

SECTION F, Description/Specifications is amended as follows:

Delete Subsection F.48.2 in its entirety and substitute therefor:

"Test for Operational Life:

The expected operating life for the production BL-LPL Assemblies shall be determined by calculation using the operating temperature and silicon device life-versus-temperature experience curve. The mean life expectancy shall be no less than 2500 hours and this shall be confirmed by direct high RF power measurement or by calculation using direct high RF power measurement of the burnout point along with established derating procedures for microwave semiconductors. (See paragraph F.49.6)"

Delete Subsection F.49.4 in its entirety and substitute therefor:

"The contractor will subject the samples to the tests specified in paragraph 6 of this provision. The confirmatory samples and associated test report must demonstrate that all applicable requirements of these specifications have been met before the contractor will be authorized to proceed with the pilot run. This authorization will be granted by the contracting officer. At least 15 calendar days prior to the start of confirmatory samples testing, the contractor shall furnish written notification to Commander, US Army, ERADCOM, Fort Monmouth, NJ 07703, of the time and location of the testing so that the Government may witness such testing if it so elects. A copy of this notification shall be furnished simultaneously to the project engineer addressed as follows: Commander, US Army ERADCOM, ATTN: DELSD-D-PC, Fort Monmouth, NJ 07703, and the Procuring Contracting Officer, Commander, US Army Communications and Electronics Materiel Readiness Command, CERCOM, ATTN: DRSEL-PC-C-CS-2(BAC) Fort Monmouth, New Jersey 07703."

Delete in its entirety Subsection F.49.6 and substitute therefor:

Paragraph F.49.6 change to read:

"a. Randomly number all units with serial numbers 1 to 20.

b. Subject the unit to tests in accordance with the following schedule.

TEST SCHEDULE

PHYSICAL	Per Figure 1	20 each Serial #1 to 20

Modification No. P00001
Supplemental Agreement to
Contract No. DAAB07-76-C-0039

TEST SCHEDULE (Cont.)

ELECTRICAL
Group A — 20 Units, Serial #1 to 20

All units will be tested and shall meet the following RF specifications.

High Power (measured at 9.3 ± 0.3 GH_z)

Peak Power	20 kilowatts
Pulse Length	0.25 microseconds
Duty Cycle	0.001
Recovery time	
to within 10 dB of low level loss	1 microsecond
to within 6 dB of low level loss	2 microsecond
to within 3 dB of low level loss	3 microsecond
Maximum Flat Leakage	50 mw
Maximum Spike Leakage	750 mw

Low Power (measured throughout the 9.0 - 9.65 GH_z range)

Maximum Insertion Loss	1.3 dB
Maximum VSWR	1.7

ENVIRONMENTAL
Group B Temperature Cycling (non-operating) — 3 each, Serial #1, 2, 3

Units shall be cycled from 25°C to + 100°C to -55°C to 25°C for one complete cycle. Thereafter they shall meet the Group A specifications above with degradations in performance of no more than:

Recovery time Increase	1 microsecond
Insertion Loss Increase	0.3 dB
Maximum VSWR	2.0
Spike Power Increase	200 mw
Flat Power Increase	25 mw

VIBRATION (non operating)
Group C — 3 each, Serial #4, 5, 6

The units shall be securely mounted to a vibration table and subjected to simple sine vibration as follows:

(a) 0.06 inch double amplitude from 20 to 26 Hz, and 2 G minimum from 26 to 2,000 Hz.

Group C (Cont.)

(b) Logarithmic sweep from 20 to 2,000 Hz for 15 minutes per sweep.
(c) or 2.5 G minimum at 50 ± 5 Hz.
(d) 15 minutes per axis, two axes.

Thereafter they shall meet the electrical specifications as explained in Group 3, above.

SHOCK (non operating)
Group D — 3 each Serial #7, 8, 9

The units shall be subjected to three shocks in each of the two directions along each of the three mutually perpendicular axis (a total of 18 shocks). The shock level shall be 25 G with a duration of 11 ± 1 milliseconds. Thereafter they shall meet the electrical specifications as explained in Group 3 above.

HUMIDITY (non-operating)
Group E — 3 each Serial #10,11,12

The units shall be subjected to an atmosphere of 80 to 98 percent relative humidity at a temperature of -10°C to +65°C for a period of one cycle. Thereafter they shall meet the electrical specifications as explained in Group 3 above.

LIFE
Group F

a) Randomly select four samples from Serial #13 thru 20.

b) Set the pulse width at 1 microsecond and a duty cycle of 0.001.

c) Set the pulse power amplitude at 5KW peak and apply it to the limiter under test for at least one (1) minute to reach thermal equilibrium.

d) Increase the pulse power to 1 KW steps, remaining at each level for at least one minute to reach equilibrium before continuing to the next level.

e) Record the highest peak power level P_M that is sustained for at least one minute by each sample.

LIFE
Group F (Cont.)

f) Verify that the unit failure occured as a result of the gold-silicon eutectic (370°C) by either:

1) removing the bulk silicon element from the resonant iris and confirming the presence of a low DC resistance (less than 100 ohms) thru the sample.

2) or locating the alloy fault thru a "lap and stain" evaluation.

g) The level obtained in step e) shall be at least 5.5 KW peak.

SECTION H, Deliveries or Performance is amended as follows:

SLIN 0001AB, Confirmatory Samples, delete "23 Dec 77" and substitute the following therefor: "17 July 1978"

SLIN 0001AC, Pilot Run, delete "25 June 78" and substitute the following therefor: "19 January 1979".

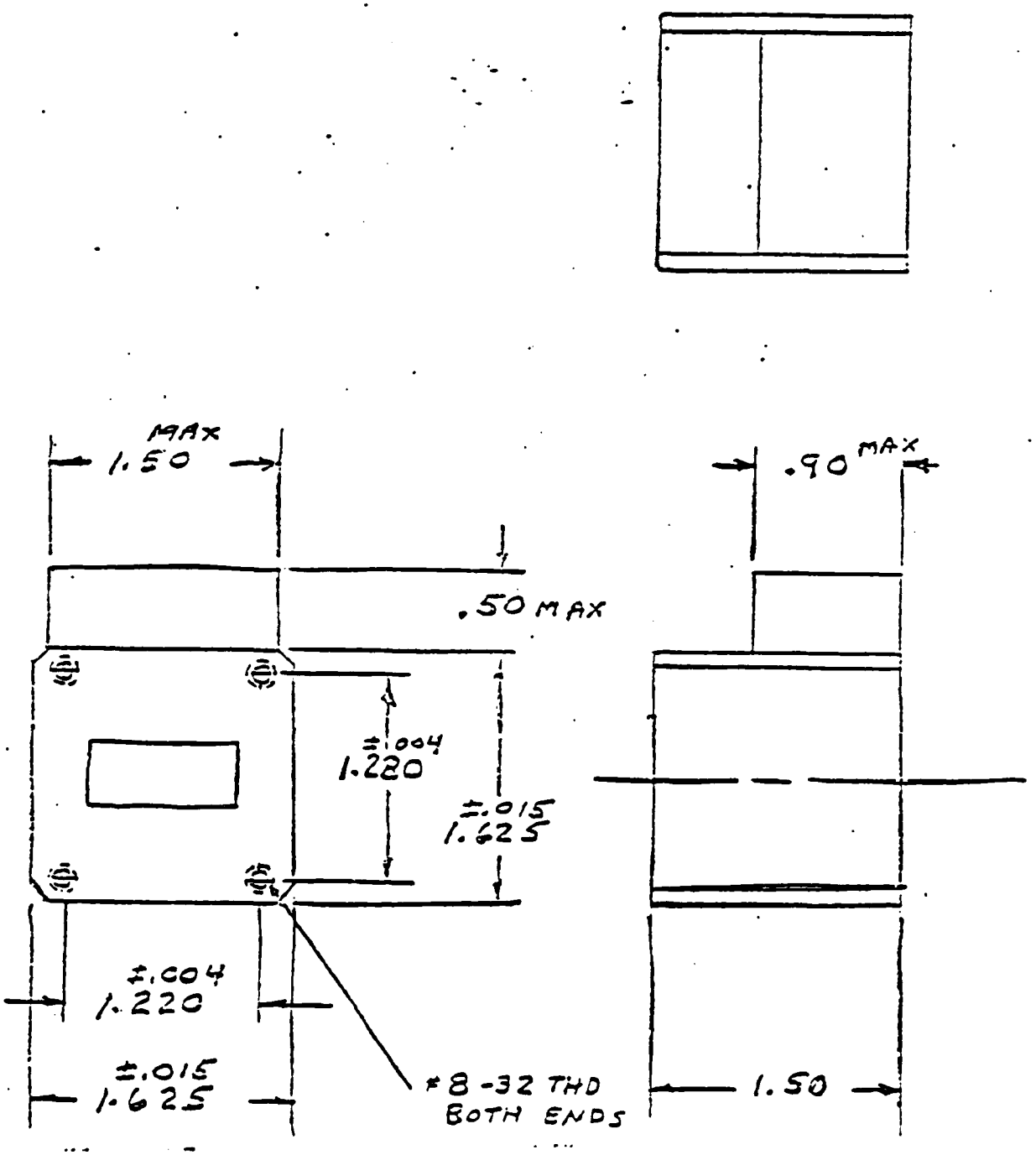

MAX
1.50
.90 MAX
.50 MAX
±.004
1.220
±.015
1.625
±.004
1.220
±.015
1.625
#8-32 THD
BOTH ENDS
1.50

FIGURE 1

APPENDIX II

QUALITY CONTROL MANUAL

MANUFACTURING SPECIFICATION

MICROWAVE ASSOCIATES, INC., BURLINGTON, MASS.

DM 960 | 1

SHT 1 OF 4

TITLE: OPERATING INSTRUCTIONS FOR M.B. VIBRATOR M/A 16-54-1

DRAWN | DATE

CHECKED | DATE

APPROVED | DATE

1.0 Purpose

This procedure outlines the test methods to be used in the operation of the MB Vibrator system, Microwave Associates Serial Number MA 16-54-1.

2.0 Operating Procedure

2.1 Mount specified control accelerometer on test jig in the plane of vibration and connect to external control loop.

2.2 Check 3-phase power lights to insure they are on.

2.3 Push green "START" button (#1) and position Plate Adjust switch (#2) to the up ( ) position on ENDEVCO power supply, Model #2623. Switch power supply on.

2.4 Switch red control (#3) on automatic Sine Programmer to the "BYPASS" position.

2.5 Turn Operation Switch (#4) to the "Scanning Off" position and turn Meter Switch (#5) to the "Power Freq. Beat" position.

2.6 Position the Frequency Range control (#6) on the "5-5000" position. Place compressor speed control (#7) on "Standard". Place output switch (#8) on the "Linear" position. Place Velocity Generator response control (#9) on "Flat" position.

2.7 Place Frequency Scanner (#10) on 60 cycles/second. Observe motion of vibration meter (#11) and adjust frequency scale adjustment (#12) until meter needle is observed to have its slowest motion with greatest displacement.

2.8 Move Meter Switch (#5) to the "Vibration Level" position.

2.9 Set Function Selector (#13) to the desired program. NOTE: If auto D-A is used the crossover point is adjusted using the control (#14). Set Frequency Scanner (#10) for desired crossover frequency and adjust center control (#14) until acceleration light (#15) "just turns on". Vary frequency scanner to insure correct operation at crossover.

2.10 Set Displacement-Velocity Range control (#15) for "Vel-Gen".

2.11 Set acceleration Range control (#17) for a g - level greater than or equal to the maximum needed for program using Accel. Gen side of the control.

2.12 Set Amplitude Control (#18) to "5"

2.13 Set Frequency Scanner (#10) to desired frequency point.

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2.0 Operating Procedure - continued

2.13

2.13.1 If program is of a frequency scanning nature, adjust maximum and minimum frequency positions with the two sliding knobs on frequency scanner (#10). Convert maximum and minimum frequencies to degrees using outside scale and figure traverse of program in degrees/minimum.

2.13.2 Set Scanning Speed (#19) and Scanning Speed Selector (#20) for desired scan.

2.14 Turn Output Voltage Control (#21) clockwise untial a "click" is heard and the "Danger Do Not Switch" lamp (#22) goes on.

CAUTION: This red light means no "Red" controls may be turned or readjusted without causing serious damage to the equipment

2.15 Check meter control (#23) to insure that it is in the .3 position.

2.16 Move Output Voltage Control (#21) slowly clockwise until a vibration level has been indicated on meters (#11) and (#24). Continue moving Output Voltage Control clockwise and observing meter for compressor suppression until knob is fully clockwise.

2.17 Set Acceleration level control (#26) to desired acceleration level as indicated on Meter (#24)

2.17.1 For D-A program - Set frequency scanner to frequency just before crossover to constant acceleration and set desired acceleration level with Displacement Level Control (#25).

2.17.2 Set Operation Switch to "Scanning On" position and monitor program on Meter (#24).

NOTE: IF ANY DIFFICULTY ARISES DURING VIBRATION

TURN OUTPUT VOLTAGE CONTROL (21) TO THE OFF

POSITION (FULLY COUNTERCLOCKWISE).

3.0 Turn-Off Instructions

3.1 Turn Both Displacement Level Control (#25) and Acceleration Level Control (#26) fully counterclockwise.

3.2 Turn Output Voltage Control (#21) fully counterclockwise, make sure red light (#22) is off.

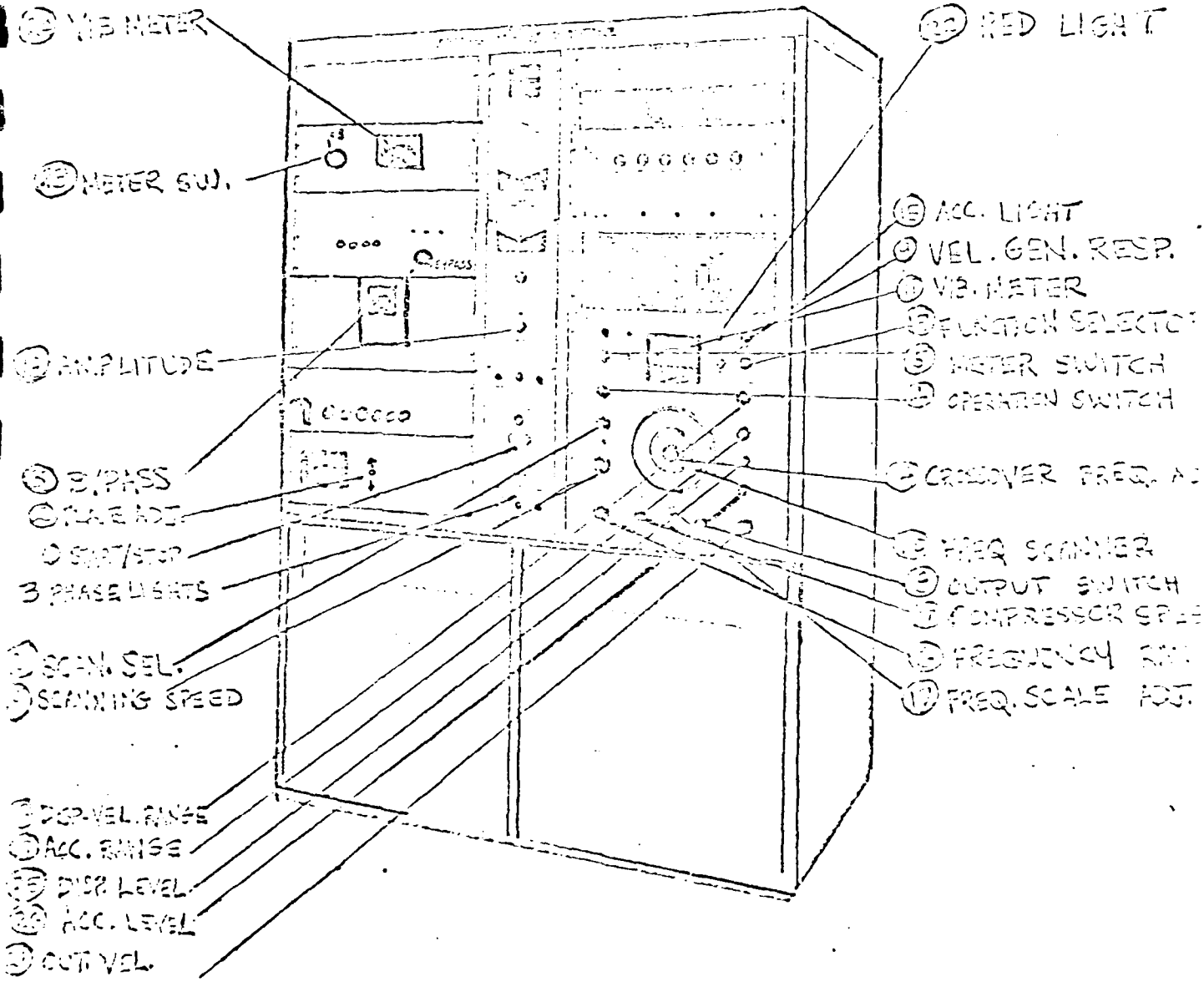
3.0 Turn-Off Instructions - continued

3.3 Turn Operation Switch (#4) to the "Scanning Off" position.

3.4 Turn Amplitude control (#8) to "0".

3.5 Push red "STOP" button.

NEW MB VIBRATOR CONTROLS



MANUFACTURING SPECIFICATION SPECTRAVE ASSOCIATES, INC., BURLINGTON, MASS.	DOC. MM 515	REV. 3
TITLE Blue M Dual Chamber THERMAL SHOCK (TEMPERATURE CYCLING)	SHT. 1 OF 6	
PRODUCT		

1.0 PURPOSE

1.1 This instruction describes the procedure to conduct thermal shock tests to MIL-STD 202, Method 107 and MIL-STD 883, Method 1010 to determine the resistance of a part when exposed to extremely low and high temperatures.

2.0 SCOPE

2.1 This instruction shall apply to products tested in the Quality Control Environmental Lab.

3.0 MATERIAL AND EQUIPMENT

3.1 Dual Chamber Thermal Test Cabinet. (Blue M Model #WSP-1090C-3)

3.2 Heat Resistant Pad/Gloves

3.3 10 inch Crescent Wrench

3.4 Liquid Nitrogen (4100 cu. ft. Tank-Suburban Welders, or equivalent)

3.5 Test Specimens

3.6 Test Trays

4.0 PROCEDURE

4.1 Connect 2 full 4100 cu. ft. tanks, to hose lines and open test valves. Hoses must be connected to Liquid Withdrawal Ports only.

4.1.1 Open Liquid Withdrawal Test Valves.

4.2 Open both Jamesbury hand valves.

4.3 Place diodes in test trays as required.

4.4 Place loaded test trays on shelves inside chamber.

4.4.1 Allow air to flow over and under each tray.

4.5 Record information of lot on Esterline Angus #400 S 3 recorder as noted on card on front of chamber.

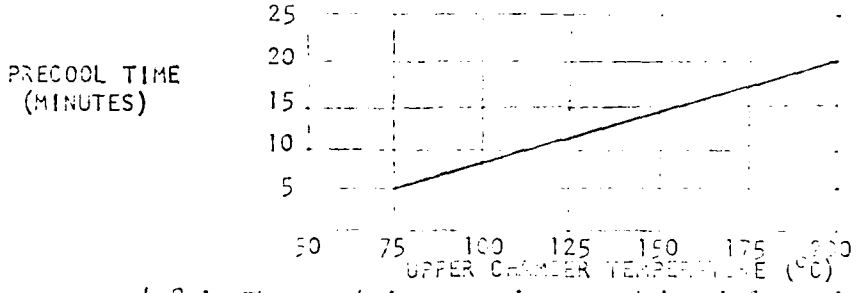
4.6 Set PDM-75 control to 25°C.

4.7 Turn the transfer timer switch to off position.

4.8 Set the precool and transfer timers as follows:

Precool timer.....Prechills the lower chamber before the elevator leaves the upper chamber. The precool period is adjustable from 2 to 55 minutes.

The approximate proper setting for the precool timer can be determined from the graph below.



4.8.1 The graph is approximate and its information must not be construed as final. Several parameters will affect the precool timer setting. Among these are the mass of the workload and the time the elevator is in the upper (heat) position.

4.8.2 The precool times shown on the graph above are a guide when performing MIL-202D, Method 107C, Steps A, B, C, if.

4.8.3 The precool timer should never be set for more than 2/3 of the time that the elevator is in the upper position. Example: If the program requires 1/2 hr. in the upper chamber, the precool timer should not be set for more than 20 minutes.

4.8.4 The precool timer should always be set for the MINIMUM amount of precooling necessary.

The precool timer is located inside the console cabinet. The time setting is determined by the angular spacing between the two arms carried by the timer's motor shaft.

To set the timing, pull the top arm outward and turn to the new setting. Upon releasing the arm, a spring locks the two arms together.

Transfer Timer.....Determines the position of the elevator. To set the timer, proceed as follows:

Set the "OFF" arm (right) for the time the elevator must be in the lower chamber, PLUS the delay set on the precool timer.

Set the "ON" arm (left) for the time the elevator must be in the upper chamber, MINUS the delay set on the precool timer.

EXAMPLE:

Desired program requires:
(a) 1 hr. in upper chamber (heat)
(b) 1 hr. in lower chamber (cold)
(c) Lower chamber to be precooled for 15 minutes

Set Flexotpulse "ON" arm for one (1) hour and 15 minutes.
Set "OFF" arm for 45 minutes.
Set precool timer for 15 minutes.

UNIT WILL NOW OPERATE as per desired program.

4.8.5 TIMER INDICATOR POINTER

4.8.5.1 Move the timer indicator pointer to the right until it makes contact with the "On" timer arm.

4.8.5.1.1 Due to the timer's internal locking device, it may be necessary to move the pointer to the extreme left, ie., making contact with the "Off" timer arm and then moving it to the extreme right.

4.8.5.2 Carefully move the timer indicator pointer to a point JUST LEFT OF CENTER. The elevator will now be in the upper position.

4.9 Set the cycle counter to the desired number of cycles plus one. ie., Cycle Counter = # of cycles +1.

4.9.1 Release lock handle to set cycle counter and then retighten.

4.9.2 The cycle counter will shut the chamber off after the last desired hot cycle and the elevator will remain in the hot chamber.

4.9.3 Cycle counter does not need to be reset from zero position.

4.10 Turn the main curcuit breaker on.

4.11 Turn the coolant switch on.

4.11.1 This switch must be "On" in order to perform thermal shock tests.

4.12 Turn the transfer timer switch on.

4.12.1 Transfer Timer Switch....Used for initial precooling or heating of the appropriate chamber.

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4.12.1 (CONTINUED)
NOTE: THIS UNIT IS DESIGNED FOR THERMAL SHOCK TESTING ONLY AND CANNOT BE USED FOR SUSTAINED TESTING AT EITHER TEMPERATURE EXTREME.

4.13 Press in reset cycle timer switch.

4.13.1 The chamber will now start and will perform desired number of cycles, and automatically shut off.

4.14 Versatronik (Honeywell) - Main Coldchamber control.

4.14.1 Set the control to the desired cold temperature by depressing and turning the knob on the front of the Versatronik (Honeywell) Control.

4.14.2 When the knob is released, the meter serves as a temperature indicator.

4.14.3 Versatronik Temperature Control....Maintains temperature of lower chamber.

When the meter face emits a red glow, this indicates that the oven temperature is above the setpoint and the coolant solenoid valve is energized. (The coolant pilot light will also indicate coolant solenoid valve operation) A green glow indicates an oven temperature below the setpoint and the coolant solenoid valve is de-energized.

The red pointer is merely an adjustable reference indicator of setpoint temperature. IT DOES NOT AFFECT TEMPERATURE!

4.15 After precool is completed and the chamber shelf has moved into the bottom section, set PCM-75 control for the desired upper chamber temperature.

4.15.1 Overtemperature Protection(OTP)....Provides protection for the chamber workload. In event of an above setpoint temperature, the OTP, control will trip, shutting the chamber off. To operate the OTP, set it approximately 5°C, (9°F.) higher than the setting on the Process-O-Matic 75 (hot chamber)control. Then, firmly press the black reset button.

4.16 Watch temperature indicator on esterline Angus Chart Recorder.

4.16.1 Make fine adjustments of hot (FDM-75) and cold (Tenstatronik) chamber controls to produce the proper test temperatures.

4.17 As noted in 4.13.1, chamber will operate until the required number of cycles are completed, and then automatically shut off.

4.18 At completion of test check Esterline Angus Recorder to determine that the number of cycles and temperature extremes were correct.

4.19 Remove test trays from chamber.

4.19.1 Use pad/Gloves if trays are still hot.

4.20 Return FDM-75 to +25°C.

4.21 Set Transfer Timer switch to off position.

4.22 Close off liquid nitrogen test valves.

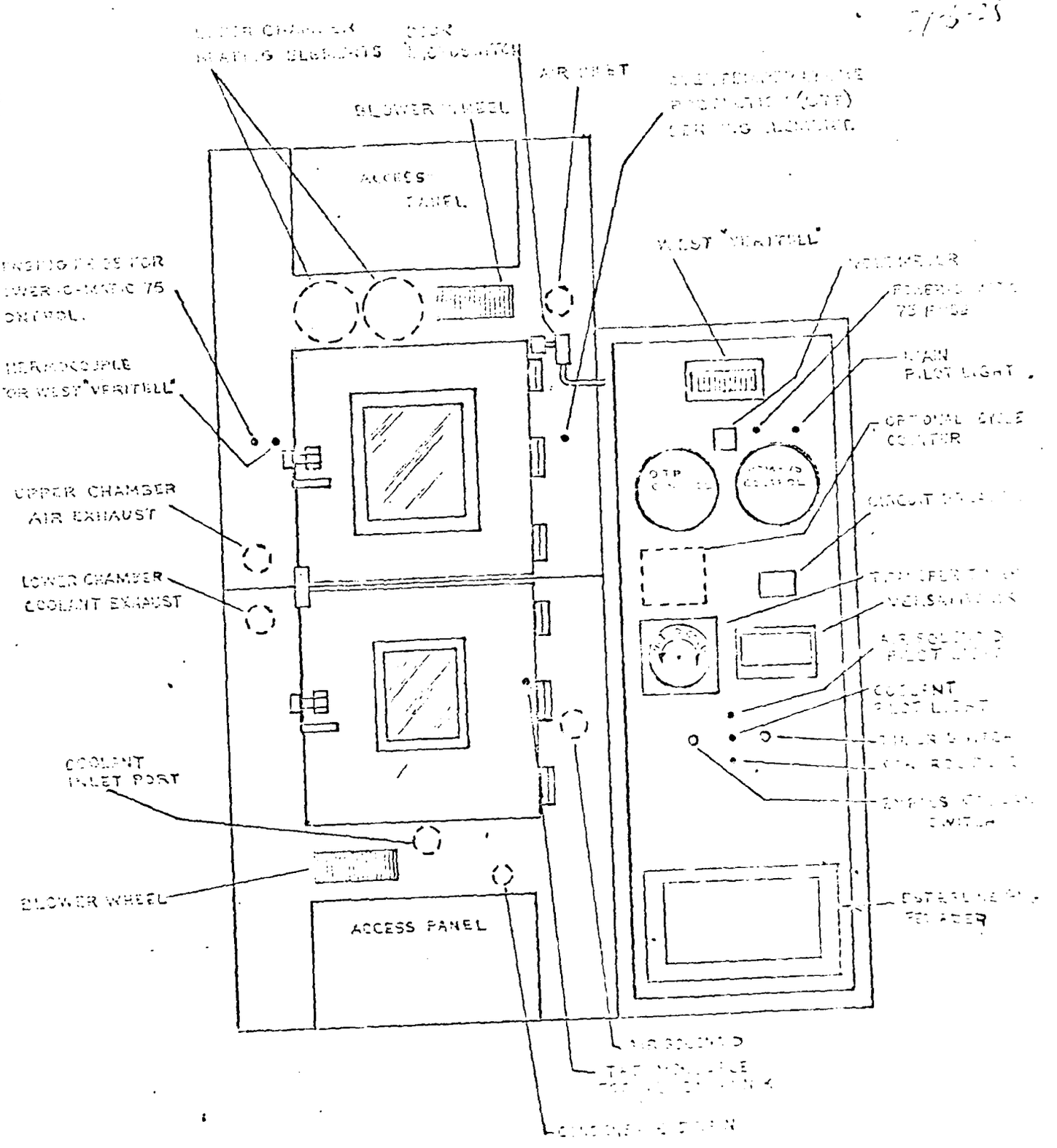
5.0 PRECAUTIONS

5.1 Avoid injury while exchanging liquid nitrogen tanks.

5.2 Do not allow liquid nitrogen to flow on skin.

5.3 Use pad /Gloves when removing specimens from the chamber.

CHAMBER FRONT VIEW



	MANUFACTURING SPECIFICATION MICROWAVE ASSOCIATES, INC., BURLINGTON, MASS.	NO. TM 904 SHEET 1 OF 3
FOR SPEC. DEPT USE ONLY	TITLE MECHANICAL SHOCK TESTING INSTRUCTION	CH NO. DATE
APPROVALS	PRODUCT VARIOUS	APPROVED DATE

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SCS2

1.0 PURPOSE

1.1 This instruction describes the procedure required to perform the shock test specified in MIL-STD-750 Method 2016 and MIL-STD-202 Method 213. In the event of conflicting requirements, the Military Specification shall govern.

2.0 SCOPE

2.1 This instruction applies to all products tested in the Quality Control Environmental Lab.

3.0 MATERIAL AND EQUIPMENT

3.1 Shock test fixture, per appropriate outline drawing (CD-S)

3.2 Test specimens

3.3 Shock tests (LAB Serial #14873) or equivalent.

3.4 Shock pads

3.5 HP oscilloscope Model No. 141B.

3.6 Endevco accelerometer type 2A02.

3.7 Power supplies, scope, etc. if required.

3.8 Craftsman torque wrench model #944643 or equivalent.

4.0 PROCEDURE

4.1 Set-Up

4.1.1 Check the applicable specification and determine the required "G" level, number of shock pulses, pulse shape and axes (Figure 1) to be tested.

4.1.2 Insure that the proper shock pads are installed on the shock tester.

4.1.3 Insure that the shock tester guide rods are clean. Do not apply oil or grease on guide rods. (Clean with trichlorethylene)

4.0 PROCEDURE (Continued)

4.1 Set-Up (Continued)

4.1.4 Adjust drop height as determined using HP oscilloscope and Endevco accelerometer.

4.1.5 Clear the area around the shock pad and test carriage.

4.2 Operation

4.2.1 Mount test specimens in the test fixture.

4.2.2 Mount the test fixture securely to the test carriage.

4.2.2.1 Torque to approximately 100 inch pounds or as determined from pulse shape.

4.2.3 Set test carriage in motion.

4.2.4 Shock test the specimens and monitor the number of shock pulses.

4.2.5 Shut off shock machine after required number of shock pulses.

4.2.6 Unload the test specimens from test fixture.

4.2.7 Repeat steps 4.2.1 through 4.2.6 as required for additional orientations.

5.0 CAUTIONS

5.1 Stand clear of the shock tester while in operation.

5.2 Insure that the test carriage does not strike the shock pad more than once for each desired shock below.

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ORIENTATION AXIS

DIRECTION OF FORCES (AS INDICATED)

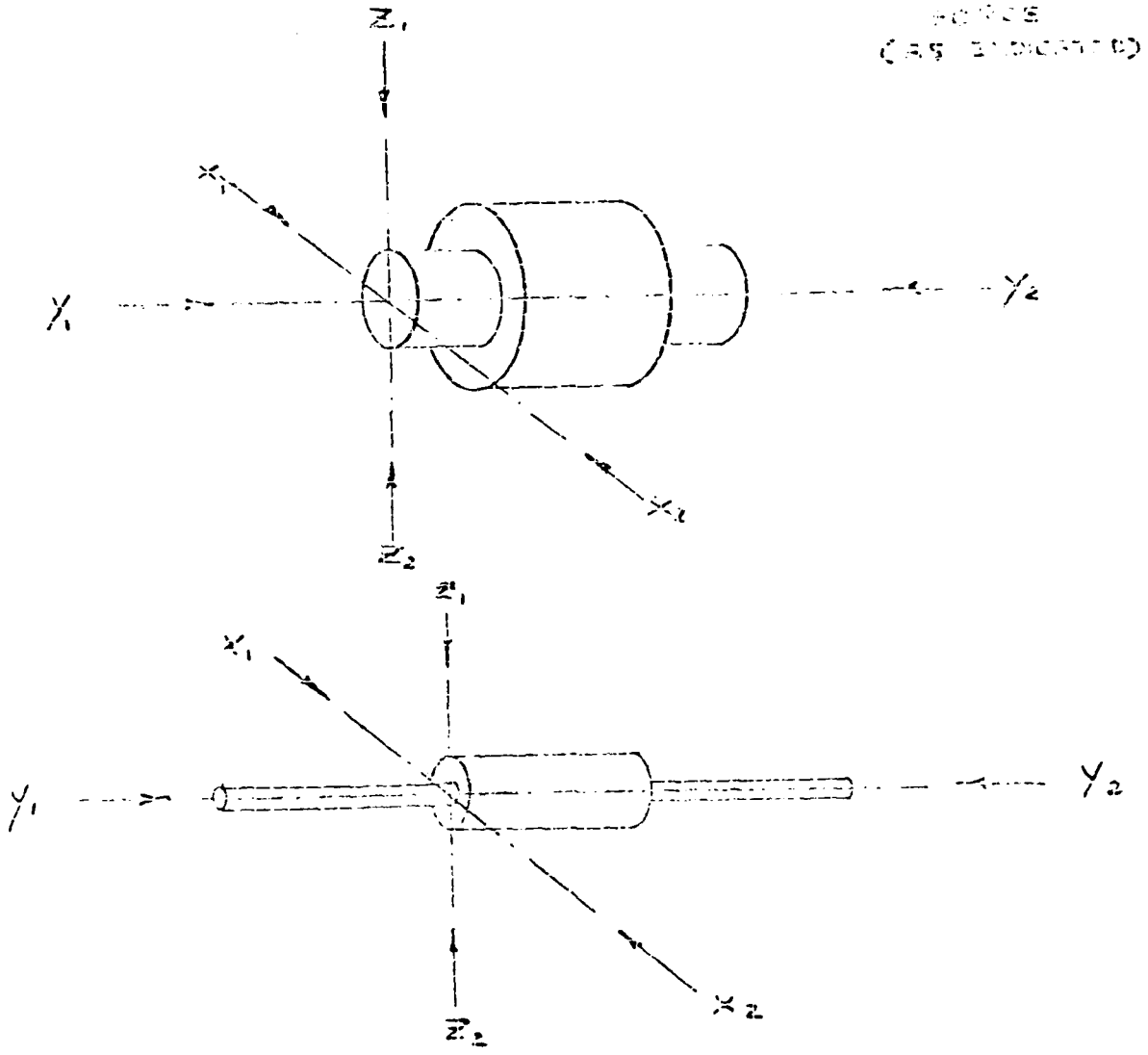

Fig. I

REVISIONS	TOLERANCES UNLESS SPECIFIED .XXX = ±.005 .0XX = .005 XX = ± .02 ANG = ½°		
DRAWN BY [illegible]	DATE [illegible]		TITLE
MATERIAL		ENGINEERING SKETCH	
USED ON Qaz 5.2.1			SK-

	MANUFACTURING SPECIFICATION MICROWAVE ASSOCIATES, INC., BURLINGTON, MASS.	NO. TM 505	
	TITLE MOISTURE RESISTANCE TEST INSTRUCTIONS	SHEET 1 OF 2 CN NO. 5276	DATE 11-13
	PRODUCT VARIOUS	APPROVED	DATE 11-13

1.0 PURPOSE

1.1 This instruction describes the procedure required to perform the moisture resistance test specified in MIL-STD-750 Method 1021 and MIL-STD-202 Method 106. In the event of conflicting requirements the Military Specification shall govern.

2.0 SCOPE

2.1 This instruction applies to all products tested by Quality Control.

3.0 MATERIAL AND EQUIPMENT

3.1 Moisture Resistance Chamber, Blue M, Model FR-250TB or equivalent.

3.2 Test specimen holder (non-corrosive).

3.3 Recorded charts (U.S. Gauge #12167) or equivalent.

3.4 Cams, cut to duplicate chart of Figure 106-1 of MIL-STD-202, Method 106.

4.0 PROCEDURE

4.1 Set-Up

4.1.1 Ensure that the water level in the reservoir tank is at least 6 inches above the top of the pump.

4.1.1.1 Use only distilled water.

4.1.2 Perform initial conditioning when required in accordance with MIL-STD-750 Method 1021.

4.1.3 Ensure that the ink supply in the recorder arm is adequate.

4.1.4 Install recording chart and record lamp.

4.1.4.1 The recording chart shall be changed daily at the beginning of each day except weekends.

4.0 PROCEDURE (Continued)

4.1 Set-Up (Continued)

4.1.5 Ensure that the proper control cam is installed.

4.1.6 Place test specimens in test chamber.

4.1.7 Place "Main" switch to "On" and ensure that indicator light is on.

4.1.8 Set "High-Low" switch to high.

4.1.9 Ensure that the switches for wet bulb, compressor and dry bulb are in the "On" position.

4.1.10 Set the "-10, + 25°C" switch to whichever temperature is required during the first 5 cycles of the test and reverse the position for the last 5 cycles.

4.1.11 Monitor operation of equipment daily, during 10 day cycle.

APPENDIX III

INITIATE

FOR SPEC. DEPT. USE ONLY

APPROVALS

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	SHEET 1 OF 4	
TITLE BULK LIMITER - TEST PROCEDURE	CN NO. 9305	DATE 79-4-24
PRODUCT BULK LIMITER	APPROVED	DATE 79-4-24

REV.

33A26433-01 thru -19 Rev. X1 and General Spec 63A24952 Rev. X2

33A26433-01FA thru 36A26433-19FA are Unscreened Types

MA45817FA thru MA45832FA.

33A26433-01BA thru 36A26433-19BA are screened types (Pre JAN TX)
MA45817BA thru MA45832BA.

MATERIAL/PVD -
ASSEMBLY/PVA - Gold Ribbon with Min. cross section 1.25 sq. mils.

OUTLINE: OD-S-31 except flange DIA. = .124" Max and over all height = .095" Max. Cathode heat sink.

TIR ≤ .005 add
Cap Concentricity ≤ .001 add

DIODE MARKING: "26433-Dash No." and Polarity Symbol

MIN CONTAINER MARKING: "33A26433-Dash No."; Date Lot Code;
96341-MA Type No.; Serial No.

TRACEABLITY - Required for a 2 year period.

CERTIFICATE OF COMPLIANCE REQUIRED WITH EACH SHIPMENT.

NOTE 1: SCREENING DATA

The manufacturer shall provide a copy of the screening variables data. Data shall be correlatable to the device part number, lot date code, and individual device serial number. The minimum data provided shall be:

a. A copy of the lot history showing compliance with or an entry on the certification of compliance to this effect.

b. A copy of the delta calculations

c. A copy of the final electrical measurements.

MANUFACTURING SPECIFICATION

MICROWAVE ASSOCIATES, INC., BURLINGTON, MASS.

NO. MA45817B/F-MA45832B ISSUE F

SHEET 2 OF 4

TITLE BULK LIMITER - TEST PROCEDURE

CN NO. 9305 DATE 79-4-24

PRODUCT BULK LIMITER

APPROVED DATE 79-4-24

REV.

FOR TYPE MA45817B THRU MA45832B ONLY

TABLE 1

100% SCREENING

(PER JAN TX REQ'MTS)

TEST	CONDITIONS 1/	SYM	MIN	MAX	UNIT
Hi Temp Life:	Method 1032 TA = 175°C	t:	24	—	Hrs.
Temp. Cycle:	Method 1051 Cond. C 10 cycles Max Temp 175°C t = >15 Min.				
Constant Acceleration:	Method 2006 Y1 Axis, 10,000G's				
Fine Leak:	Method 1051 Cond. H	LR:	—	$5X10^{-7}$	cc/sec
Gross Leak:	Method 1051 Cond. C				

READ AND RECORD C_T4, $V_{(BR)}$ AND I_R PER TABLE 11.

Burn-In:	Method 1038 Cond. A V_R = 36 ± 2 Vdc TA = 150°C	t:	96	—	Hrs.

READ AND RECORD C_T4, $V_{(BR)}$ NA I_R PER TABLE 11.
WITHIN 24 HOURS AND THE FOLLOWING DELTAS APPLY:

$\Delta C_T4 = \pm 1.0\%$

$\Delta V_{(BR)} = \pm 10\%$

$\Delta I_R = \pm 50nA$

FINAL ELECTRICAL MEASUREMENTS TESTS #1-6 AND #4 @ 25°C ONLY PER TABLE 11.

READ AND RECORD DATA

TABLE 11

(T_A = 25°C UNLESS OTHERWISE SPECIFIED)

TEST	CONDITIONS 1/	SYM	MIN	MAX	UNIT
1. Total Capacity:	Method 4102 f = 1 MHz V_R = -4V	C_T4:	SEE TABLE III		pF
2. Capacitance Ratio: See Note 2	Method 4102 f = 1 MHz V_R = 0V V_R = -45V	C_T0/C_T~~45~~25:	SEE TABLE III		---
3. Quality Factor:	Method 4036 f = 50 MHz 1/ V_R = -40V	Q:	SEE TABLE III		---
4. Reverse Leakage Current:	Method 4016 V_R = ~~-25V~~ 36V -55°C ≤T_A≤125°C	I_R:	---	20 nA	~~DAY~~
5. Reverse Breakdown Votlage:	Method 4021 I_R = 10 µA	$V_{(BR)}$:	45	---	Volts
6. Parallel Resistance:	Method 4036 V_R = 0 AC test voltage =75mV (RMS)	R_{PO}:	10	---	Mohms
7. Temp. Coefficient of Capacity:	Method 4102 f = 1 MHz V_R = -4V -55°C≤T_A≤125°C	TC_C:	---	300	ppm/°C
8. Thermal Resistance, Junction to Case: see Note 1	Method 4081 "Infinite" heat sink	RO~~JC~~: ~~30~~ see table III			°C/W

Note 1 Θ measured by customer using Sage "Theta 100 Kit" with K factor .486 and I = .25A - Θ measurements must be correlated with Omni Spectra standards before testing of each lot.

For Engr Info → Note 2 "Gamma" must be equal to min

INITIATED	MANUFACTURING SPECIFICATION	NO. MA45817B/F-45832B/F	ISSUE /
CHECKED	MICROWAVE ASSOCIATES, INC., BURLINGTON, MASS.	SHEET 4 OF 4	
FOR SPEC. DEPT. USE ONLY	TITLE BULK LIMITER - TEST PROCEDURE	CN NO. 9305	DATE 79-4-24
APPROVALS	PRODUCT BULK LIMITER	APPROVED	DATE 79-4-24

O=.7
M=.455

TABLE 111

CAPACITANCE, CAPACITANCE RATIO AND Q VALUE

add

DASH NO.	add C1	MA NO.	TOTAL CAPACITANCE CT4 pF MIN	MAX	CAPACITANCE RATIO CTO/CT25 MIN	add OC/W Q MAX	Q VALUE MIN
-01	.7-.89	MA45817*	~~0.30~~ .410	0.490	2.36	50	3000
-02	.9-1.10	MA45818*	~~0.50~~ .494	~~0.69~~ .571	~~2.3~~ 2.68	50	3000
-03	1.11-1.34	MA45819*	~~0.70~~ .583	~~0.89~~ .670	~~3.3~~ 2.95	50	~~2800~~ 2600
-04	1.35-1.5	MA45820*	~~0.90~~ .683	~~1.10~~ .746	~~3.9~~ 3.19	50	~~2800~~ 2600
-05	2.6-2.99	MA45821*	~~1.11~~ 1.209	~~1.32~~ 1.373	~~4.3~~ 3.90	45	~~2600~~ 2400
-07	3.0-3.4	MA45822*	~~1.33~~ 1.37	~~1.65~~ 1.55	~~4.6~~ 4.04	45	2400
-08		MA45823*	1.66	1.98	4.9		2300
-09		MA45824*	1.99	2.42	5.1		2200
-10		MA45825*	2.43	2.97	5.2		2200
-11		MA45826*	2.98	3.63	5.3		2100
-13		MA45827*	3.64	4.29	5.4		2000
-14		MA45828*	4.30	5.17	5.4		2000
-15		MA45829*	5.18	6.16	5.5		1900
-16		MA45830*	6.17	7.48	5.6		1800
-17		MA45831*	7.49	9.02	5.7		1700
-19		MA45832*	9.03	11.0	5.8		1600

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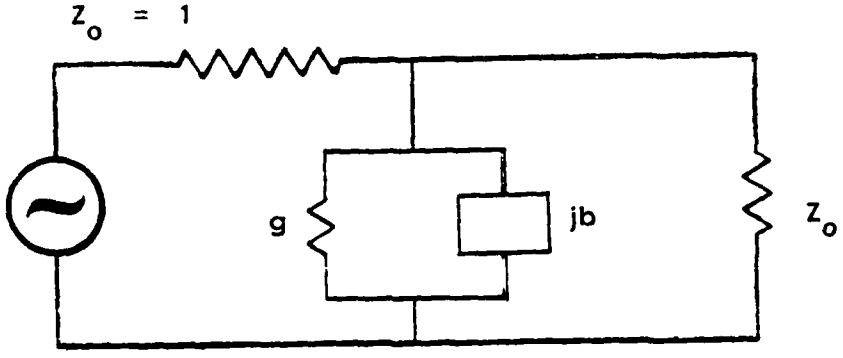
* ADD LETTER F FOR UNSCREENED TO PART NUMBERS.

* ADD LETTER B FOR JAN TX SCREENING TO PART NUMBERS.

APPENDIX IV

Using relation (from Reference 11):

$$IL = \left| 1 + \frac{Y Z_o}{2} \right|^2$$



$$Z_o = 1$$

$$Y = g + jb$$

$$\frac{Y}{2} = \frac{g}{2} + \frac{jb}{2}$$

$$\left| 1 + \frac{Y Z_o}{2} \right|^2 = \left| 1 + \frac{Y}{2} \right|^2 = \left| \left(1 + \frac{g}{2} \right) + \frac{jb}{2} \right|^2$$

$$= \left| 1 + g + \frac{g^2}{4} + \frac{b^2}{4} \right|$$

at resonance, i.e., at f_o, $jb = 0$

At low RF power and f_o, considering IL = 0.25 dB =

$$1.0593 = \left| 1 + \frac{g}{2} \right|^2$$

$$1.0292 = 1 + \frac{g}{2}$$

$$\frac{g}{2} = 0.0292$$

$$g = 0.058401$$

$$r = \frac{1}{g} = 17.12$$

$$R_T = r\, Z_o = r\ (1\ \text{ohm}) = 17.12\ \text{ohms} \quad \text{(for low power)}$$

$$\text{IL (= ISOL)} = 24.9\ \text{dB} = 309.03 = \left| 1 + \frac{g}{2} \right|^2$$

$$17.579 = 1 + \frac{g}{2}$$

$$g = 33.158$$

$$R_T = 0.03\ \text{ohm} \quad \text{(for high power)}$$

If now Z_o = 0.5 ohm (not 1.0 ohm), then:

$$IL = \left| 1 + \frac{g}{2} \right|^2$$

$$= \left| 1 + \frac{0.058401}{(2)} \times \frac{1}{2} \right|^2$$

$$= 0.1259 \text{ dB}$$

$$ISOL = \left| 1 + \frac{1}{0.03} \times \frac{1}{2} \times \frac{1}{2} \right|^2$$

$$= 87.11 = 19.4 \text{ dB}$$

$$\text{(arc loss)} = \frac{P_d}{P_i} = \frac{g}{\left| 1 + \frac{g}{2} \right|^2}$$

$$= \frac{16.667}{\left| 1 + \frac{16.667}{2} \right|^2}$$

$$= \frac{16.667}{87.111} = 0.19133$$

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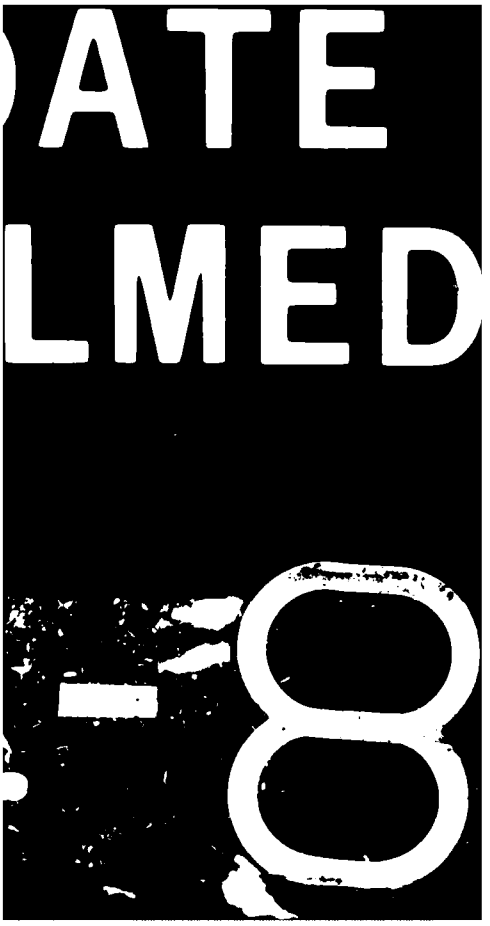
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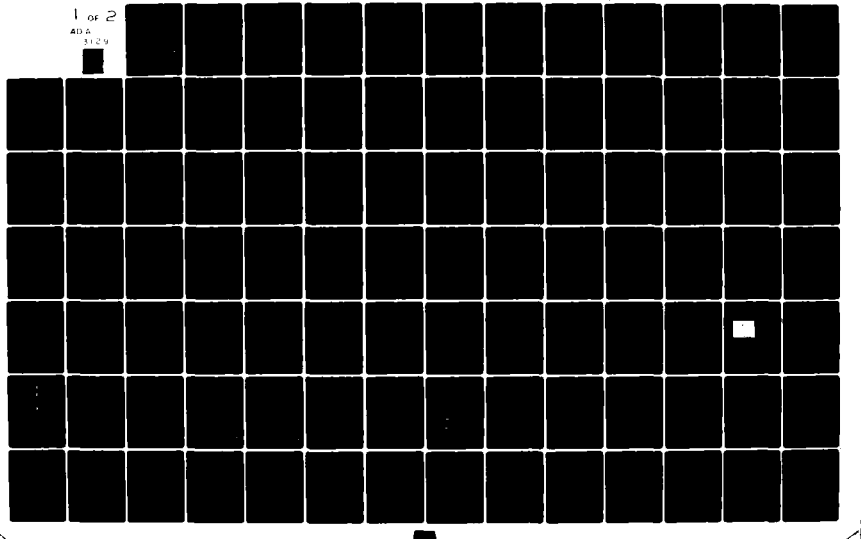

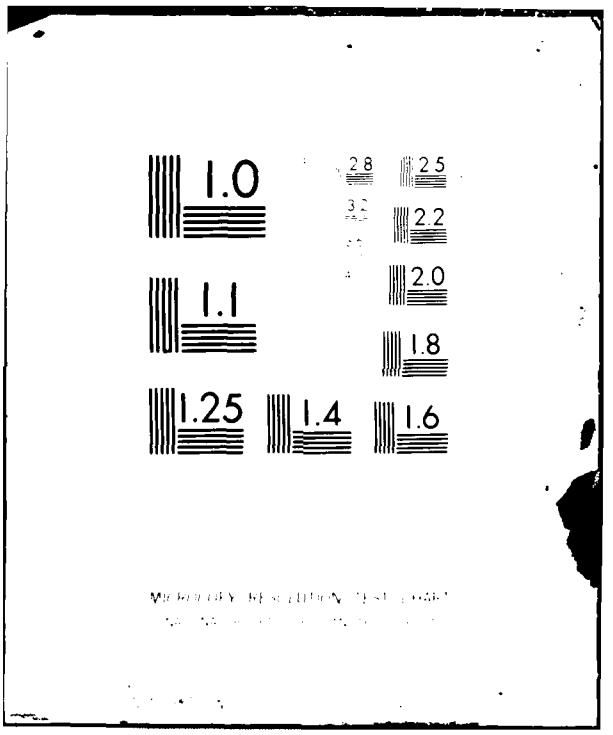
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Research and Development Technical Report
DELET-TR-76-0039

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

FINAL REPORT
JULY 1979
CONTRACT NUMBER: DAAB07-76-C-0039

Y. ANAND

MICROWAVE ASSOCIATES, INC.
Burlington, MA 01803

Prepared for:
US ARMY ELECTRONICS TECHNOLOGY & DEVICES LABORATORY

ERADCOM
US ARMY ELECTRONICS RESEARCH & DEVELOPMENT COMMAND
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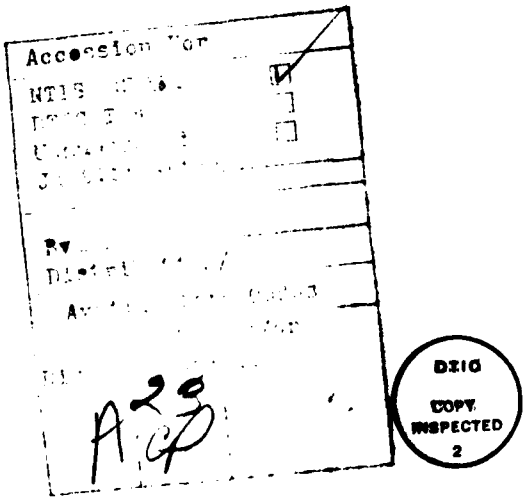

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July, 1979

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MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH POWER BULK SEMICONDUCTOR LIMITERS

FINAL REPORT

JULY, 1979

CONTRACT NUMBER: DAAB07-76-C-0039

Distribution Statement

Approved for public release; distribution unlimited

Objective of Study

To establish the capability to manufacture "High Power Bulk Semiconductor Limiters" at X-band frequencies per Electronic Command Development Description, DAAB07-76-C-0039, on a pilot line including actual fabrication of test samples and a production run.

Prepared By:

Y. Anand

MICROWAVE ASSOCIATES, INC.
Burlington, Massachusetts 01803

Prepared For:

U.S. ARMY ELECTRONICS TECHNOLOGY & DEVICES LABORATORY
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This report describes the Production Engineering of high power bulk semiconductor limiters for X-band frequencies. A high power bulk semiconductor limiter assembly, consisting of a high resistivity silicon bulk limiter and followed by a two-stage junction diode limiter was developed for the frequency band of 9 - 9.65 GHz. This receiver protector handles 20 kW of peak power at a 0.25 μsec pulse width and 4000 Hz pulse repetition frequency. High volume semiconductor batch processed and fabrication techniques were implemented to obtain this

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low cost and reliable receiver protector.

A pilot line was established to fabricate the bulk limiters in production quantities for reliability testing and to supply the U.S. Army with eighty-five (85) units.

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ABSTRACT

This report describes the Production Engineering of high power bulk semiconductor limiters for X-band frequencies. A high power bulk semiconductor limiter assembly, consisting of a high resistivity silicon bulk limiter and followed by a two-stage junction diode limiter was developed for the frequency band of 9 - 9.65 GHz. This receiver protector handles 20 kW of peak power at a 0.25 μsec pulse width and 4000 Hz pulse repetition frequency. High volume semiconductor batch processes and fabrication techniques were implemented to obtain this low cost and reliable receiver protector.

A pilot line was established to fabricate the bulk limiters in production quantities for reliability testing and to supply the U.S. Army with eighty-five (85) units.

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U. S. Army Electronics Command Technical requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time (2) high power capability, (3) insertion loss and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G, and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No., 15, dated December 1975, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include ion formation, circuit configuration, material characterization and chip [illegible]. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III, and IV a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually,

any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

NARRATIVE AND DATA

This Final Report, in accordance with ECIPPER, No. 15, is divided into three sections. These sections are as follows:

I Technical Program Discussions

II Complete Process Specifications

III Quality Control Environmental Test Methods

I. TECHNICAL PROGRAM DISCUSSIONS

The objective of this Manufacturing Methods and Technology Engineering program was to establish the producibility of the X-band bulk semiconductor limiter and the X-band two-stage PIN limiter by mass-production techniques. The planned production rate was the pilot line capability of one-hundred (100) bulk limiters per month.

Originally, the bulk semiconductor limiter requirements were those called for per the Electronics Command Technical requirements SCS-486 and Amendments to the specification dated 28 March 1975. Based on performance capability established by the engineering samples provided on this program, a revised production specification was established to be used for the preproduction devices for the confirmatory samples and pilot line production.

The final specification of the bulk semiconductor - limiter assembly is given in Appendix I. The pertinent specified characteristics of the limiter are listed below.

- High Power (measured at 9.3 ± 0.3 GHz)

Peak Power	:	20	kW
Pulse Length	:	0.25	μsec
Duty Cycle	:	0.001	
Recovery Time			
- to within 10 dB of low level loss	:	1	μsec
- to within 6 dB of low level loss	:	2	μsec
- to within 3 dB of low level loss	:	3	μsec
Maximum Flat Leakage	:	50	mW
Maximum Spike Leakage	:	750	mW

Low Power: (measured throughout the 9.0-9.65 GHz Range)

Maximum Insertion Loss : 1.3 dB

Maximum VSWR : 1.7

External Bias : NONE

- Absolute Rating Objectives:

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P		20	kW

About half-way through the program, a contract modification was made, also increasing the number of confirmatory samples (from limiter assemblies) from four (4) to twenty (20) units.

The overall program schedule, as was actually carried out, is given on the following page.

OVERALL PROGRAM SCHEDULE

	COMPLETION DATE
PHASE I : ENGINEERING	
• Design	September 1976
• Shipment of First Lot of Engineering Samples (five limiters, one clean-up limiter)	October 1976
• Design Improvement I Shipment of Second Lot of Engineering Samples	January 1977
• Design Improvement II Shipment of Third Lot of Engineering Samples	April 1977
PHASE II : PREPRODUCTION	
• Manufacture of Preproduction Samples	February 1978
• Approval of Test Facilities	March 1978
• Confirmatory Sample Testing	April 1978
• Delivery of Confirmatory Samples (twenty bulk limiters, 20 clean-up limiters)	July 1978
• Acceptance of Preproduction Samples and Authorization to Proceed with Pilot Line	November 1978
PHASE III: PILOT LINE	
• Preparation of Inspection and Quality Control Plan	February 1979
• Approval of Above Plan	March 1979
• Manufacture of Bulk Limiters for Pilot Run Qualification Testing and Shipment of Pilot Run (forty bulk limiters, 40 clean-up limiters)	April 1979

OVERALL PROGRAM SCHEDULE (Cont'd)

	COMPLETION DATE
PHASE III: PILOT LINE (Continued)	
• Preparation of the FINAL Report	July 1979
• Preparation of the General Report on Step II	July 1979
• Preparation of the Bill of Materials	July 1979

A. Engineering Phase

The object of this program was to establish the producibility of the X-band bulk semiconductor limiter and the X-band lower power diode multi-stage limiter by mass-production techniques. The two important goals of this Engineering Phase were:

1. Optimize the circuit design of the composite limiter to meet SCS-446 objectives.
2. Incorporate changes into the basic design developed by RRC which facilitate the manufacture and improve the production yield of production limiter components.

The complete circuit analysis, diode improvements, and final design are discussed in the next two sections.

B. Theory of Bulk Limiter Operation

1. Basic Operation

The bulk semiconductor limiter in its early stages was a piece of high resistivity silicon with two sintered or diffused ohmic contacts. The contacts were connected to a high impedance microwave transmission line circuit.[1-3] The device has since been developed with improved passivation circuit and thermal designs.[4-7] A major change in the contact surfaces of the device, checkerboard contacts, has been developed[4] which improves the isolation state performance by permitting microwave fields to cause holes and electrons to be injected into the high resistivity silicon. The new contact structure also accelerates recombination of holes and electrons after a microwave pulse has terminated; thus, it reduces the recovery time of the device to the order of one microsecond from previous values of approximately ten microseconds.

In operation at low microwave field intensities the bulk limiter element with checkerboard contacts behaves as a high Q capacitor. Thus if it is incorporated into a parallel resonant circuit shunting a waveguide, microwave signals will pass with minimal attenuation at the resonant frequency. At higher power levels the microwave electric field across the device causes both electrons and holes to be injected into the high resistivity bulk region of the device. These carriers reduce the resistivity of the bulk element and changes its characteristics from a high Q capacitor to a capacitor with shunt conductance. The table below shows conductivity values calculated from microwave limiting data of bulk limiters at 9.3 GHz as a function of rms microwave field intensity.[7]

E (V/cm)	θ (mho/cm)	ρ (ohm/cm)
100	3.33×10^{-4}	3000
1,000	1.12×10^{-3}	891
10,000	1.48×10^{-2}	67.7
20,000	4.76×10^{-2}	21
40,000	3.0×10^{-1}	3.3

The isolation state with increased conductance is a non-equilibrium state much like a PIN diode under forward bias. The major difference between the bulk limiter and a thick based PIN diode is the contacts. The checkerboard limiter can be self-biased into conduction by a microwave field while a PIN can not. For this reason a thick based PIP, NIN, or PIN structure would all be expected to perform similarly with no limiting until an avalanche field intensity is reached somewhere within the device.

2. Microwave Field Conductivity Modulation

Figure 1 shows an exploded view of a section of a checkerboard contact limiter element. Checkerboard P-N doped contacts are present on each side of the limiter element. The central region is high resistivity silicon which is typically about 3 mils thick.

Figure 2 shows the effect of applying a high level microwave field across the device. Only the top contact is shown, but it will be understood that the bottom contact functions in the same manner. In Figure 2a the excess mobile carrier distribution is shown before bias is applied; there are no excess carriers. In Figure 2b the carrier distribution as a result of the first positive half cycle is shown. Mobile carriers, holes, build up a space charge within the intrinsic material. During the negative half cycle, most of the holes are removed by the electric field. The holes near the shorted P-N junction of the contact surface are not removed, however, as their space charge is neutralized by extra electrons injected by the N doped region. This

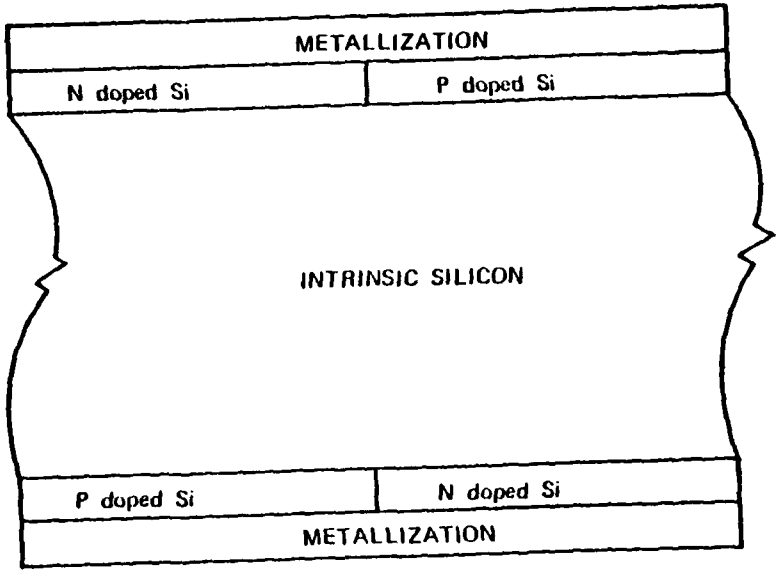


FIGURE 1 SECTION OF A CHECKERBOARD LIMITER ELEMENT

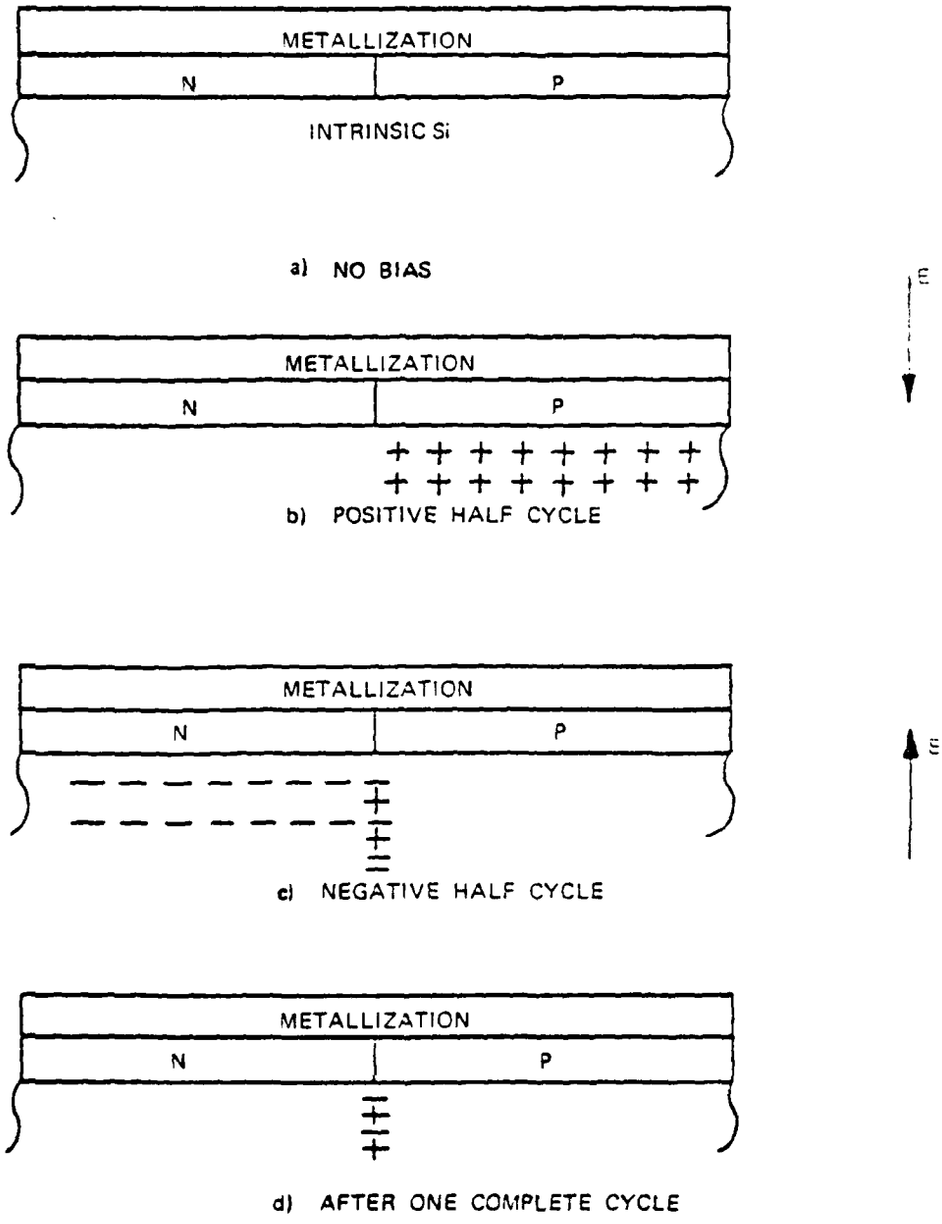


FIGURE 2 EXCESS MOBILE CHARGE DISTRIBUTION CAUSED BY HIGH LEVEL MICROWAVE

effect is shown schematically in Figure 2(c). At the end of a complete cycle the excess mobile carrier distribution is as shown in Figure 2(d).

The net effect of the checkerboard contact structure is to permit a neutral hole-electron plasma of excess carriers to be injected at the shorted surface P-N junctions in response to an applied microwave electric field. This plasma has the effect of modulating the bulk conductivity of the intrinsic region so the increase in shunt conductivity across the device terminals can be used to produce a limiting phenomenon. After a short turn-on (spike leakage) period, the plasma is distributed substantially uniformly throughout the intrinsic region of the limiter element.

3. Recovery from the Plasma Limiting State

The hole-electron plasma which causes the limiter to exhibit isolation performance is present at the end of the high power microwave pulse. After the pulse is over, the plasma must recombine or otherwise be removed from the intrinsic region before the device can return to its low level transmission state. In a PIN diode the built in electric field at the P-I interface prevents electrons from entering the degenerate P region and recombining. Also a similar field at the N-I junction prevents holes from entering the degenerate N region and recombining there.

Figure 3 shows the electric field distribution that is always present at the interface between intrinsic silicon and a checkerboard contact. Far from the shorted surface junction the fields are as they would be in a normal N-I or P-I junction; hence, little recombination occurs there. Near the shorted junction, however, a large electric field exists which drifts excess holes into the P doped contact region and excess electrons into the n doped region. This carrier flow causes an equal current to flow in the metallization layer which shorts the N and P region. The contact surface behaves very much like a shorted silicon photo cell junction. Thus, the checkerboard contact has a matrix of shorted P-N junctions whose built-in

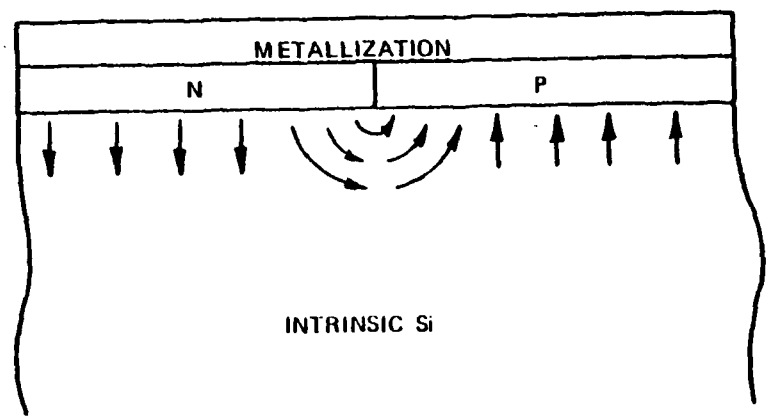


FIGURE 3 BUILT IN ELECTRIC FIELD DISTRIBUTION
AROUND CHECKERBOARD CONTACT STRUCTURE

potential recombines holes and electrons when no microwave field is present.

It is this high rate of surface carrier recombination caused by the checkerboard's shorted junctions that is responsible for the rapid recovery of the bulk limiter to the dielectric transmission state from the conductivity modulated isolation state.

C. Bulk Semiconductor Limiter Design Consideration

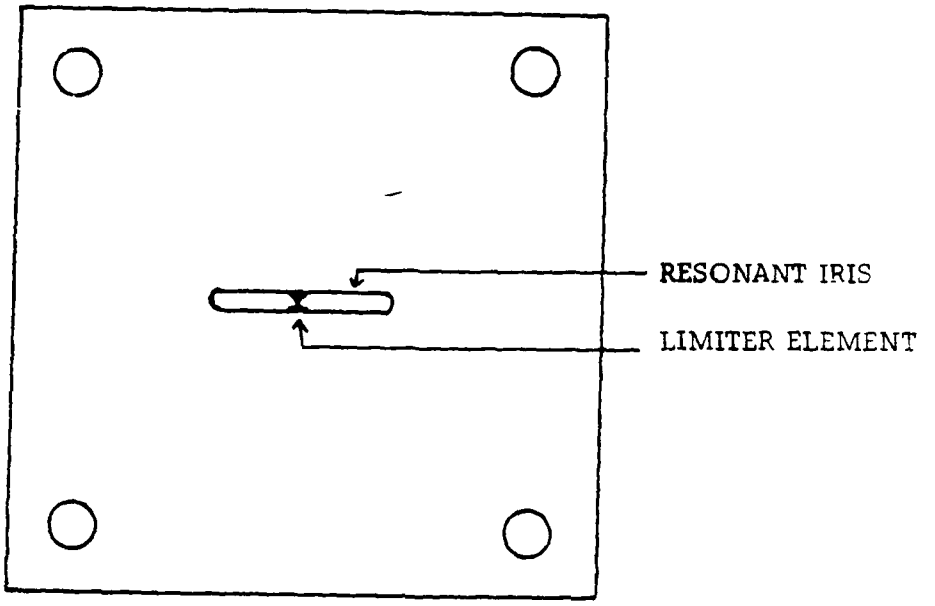
1. Introduction

The bulk semiconductor limiter is a small, lightweight, solid state device. It has good peak power capability but is limited somewhat in average power ability. It turns on very rapidly (less than 1 nsec), producing an attenuated leakage spike which is only 3 to 7 dB above the ultimate flat depending upon the construction and operating conditions.

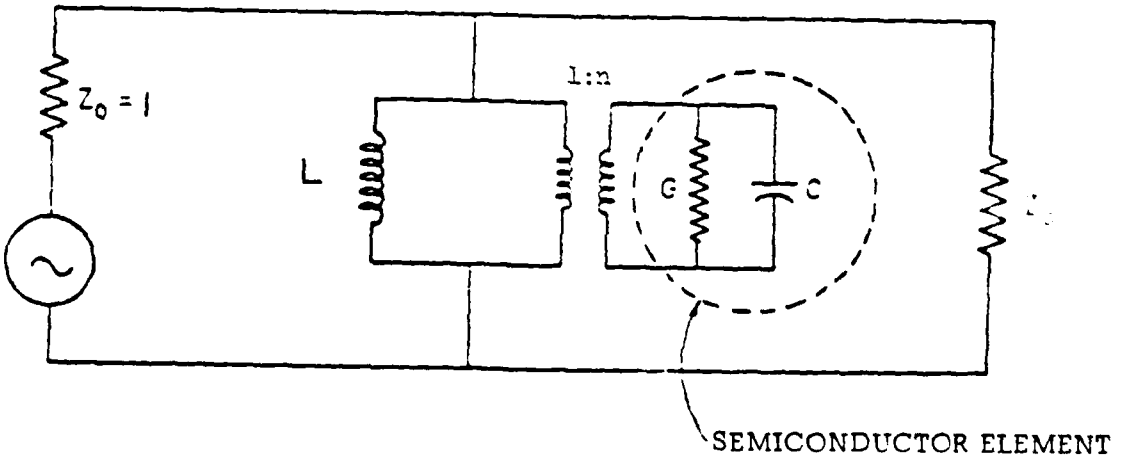
2. Choice of Circuit Structure

From basic avalanche phenomenon considerations, it is evident that to achieve appreciable nonlinearity for an applied signal, a field intensity corresponding to the threshold voltage of several tens of kilovolts/cm, would have to be obtained for a silicon limiter. Thus, a microwave structure in a waveguide which would provide a concentration of electric field across a gap of typically 10 mils is needed. Further, the circuit structure employed with the bulk limiter element should yield negligible insertion loss for low signal levels. One of the simplest structures to meet these requirements is the resonant iris.

Thus, for the purpose of evaluating basic limiting properties as well as determining the physical changes occurring in the bulk element, a horizontal slot (typically 25 x 450 mils) is used to form X-band iris. (See Figure 4). This iris in turn is simply sandwiched in between two waveguide flanges (sections) to insert the limiting component into a microwave system. The empty iris is designed to appear inductive at the operating frequency (resonant at a much higher frequency) such that the capacitive loading produced by the relatively lossless ($Q_\mu \approx 500$) silicon element placed across the center of the iris slot would yield a resonant structure. As a result, shunt losses representative of the high resistivity



a) LIMITER STRUCTURE



b) LIMITER EQUIVALENT CIRCUIT

FIGURE 4 LIMITER STRUCTURE AND EQUIVALENT CIRCUIT

silicon element (at low signal levels) and the metallic diaphragm determine the equivalent shunt conductance appearing across the waveguide and thus the insertion loss. When this circuit structure is exposed to high microwave field intensities, the bulk element becomes progressively more conductive. The transmission of power through the iris slot is thus limited, and the circuit acts primarily as a reflective termination to the incidence power.

In addition to providing the desired low and high power transmissive and reflective states, this simple structure also provides moderate 3 dB down bandwidth (typically 10%) in the low level transmission state while yielding the high field concentration at the silicon element. Further, the structure provides good thermal conductance from the element to the heat sink provided by the waveguide walls. This fact insures high power dissipation capability for long pulses and moderate repetition rates.

3. Bulk Semiconductor Limiter Design Characteristics

The derivation and basis for the equations and relationships pertaining to the electrical operation of bulk semiconductor limiters are discussed in references 1 to 8, and will not be repeated in detail here. The objective of the present section is to develop a set of limiter operating characteristics using in a simple manner the expressions developed in the previous reports.

4. Low Level Loss and Bandwidth

The limiter chip positioned in its resonant microwave iris appears as a transformer coupled shunt loading (Y) to the waveguide transmission line (Z_o). Figure 4 shows the physical limiter structure and its equivalent electrical circuit. The insertion loss (IL), which is defined as the incident power (P_{in}) divided by the transmitted power (P_t), is given by the following expression:[11]

$$IL = \frac{P_{in}}{P_t} = \left(1 + \frac{Y Z_o}{2}\right)^2 \qquad (1)$$

Inserting the circuit elements yields the expression below.[1]

$$IL = \left(1 + \frac{n^2 G}{2}\right)^2 + (2 \pi df C n^2)^2 \qquad (2)$$

where
- f = fo + df = operating frequency in hertz
- fo = circuit resonant frequency
- n = transformer turns ratio in $(ohms)^{1/2}$
  Transmission line impedance is normalized to unity.
- G = limiter element conductance in mhos
  This assumes that the dominant loss is in the silicon.
- C = limiter element capacitance in farads

Note that at resonance the last term in Equation (2) is zero. The remaining expression relates the mid band insertion loss to the element conductance, which can in turn be related to the silicon conductivity.

$$G = \sigma C/\epsilon$$

where
- σ = limiter element conductivity in mho/cm
- ϵ = dielectric constant of silicon element in farads/cm

The relation for the turns ratio (n) is the most controversial of those used in this development. The turns ratio basically represents the coupling between the resonant iris circuit and the transmission line. It is therefore dependent upon the dimensions of the iris openings. It is also dependent upon the limiter element mounting structure and its associated parasitic reactances.

If an iris of fixed height and thickness is loaded with capacitances of different values, a linear relationship is experimentally found between the square of the turns ratio and the element capacitance. Further, if all dimensions are scaled, n^2 will remain constant. Thus, the following empirical relationship results:

$$n^2 = k \quad C(pF) \quad f(GHz) \tag{4}$$

where k is a constant for a given iris type. The factor k is evaluated using experimental capacitance and bandwidth data in conjunction with Equation (2).

Using the relations presented so far, graphs can be generated relating the insertion loss and bandwidth to the element capacitance and operating frequency.

The data provided in this report is generated using the circuit shown in Figure 5. The series inductance element (LW) is added to represent the inductance of the current mounting structures which employ relatively thin wire bonded to the dot contact on the limiter element. The resistive element (R) provides for metallic losses, but these are usually small compared to those in G. The inductance (L) is transformed to the other side of the transformer in Figure 5 simply for convenience. This causes no change in the analysis.

In using the circuit of Figure 5 to calculate the turns ratio (n), the equivalent capacitance of the R-LW-G-C combination must be used in Equation (4). The low level conductance (G) and capacitance can be obtained directly from the element bulk properties and geometry. Assuming R to be negligible LW and n can be obtained from experimental data of the 3 dB bandwidth and maximum achievable (saturation) isolation. The inductance parameter (L) is adjusted to provide resonance at the frequency of operation.

At 8.25 GHz, a limiter with an element capacitance of 0.08 pF is measured to provide a 1.0 GHz bandwidth and 28 dB isolation at saturation. For these conditions, LW is calculated to be 1.18 nH and n^2 is specified by Equation (4) and LW is adjusted to provide a constant impedance. Effects due to the variation of transmission line impedence with frequency are considered of secondary importance in relation to the purposes here and are neglected.

Having thus specified all the component values of the circuit in Figure 5, the low level insertion loss is computed and presented in Figure 6 as a function of capacitance for several frequencies. As expected, higher capacitance and higher frequencies exhibit higher loss. In comparison with previous calculations, the effect of adding the LW term is to narrow the tolerable range of capacitance for a given loss range. Typical capacitance values for about 0.4 dB loss are listed below for several frequencies.

CAPACITANCE (pF)	FREQUENCY (GHz)
0.150	3.5
0.075	9.5
0.050	16.5
0.030	35.0

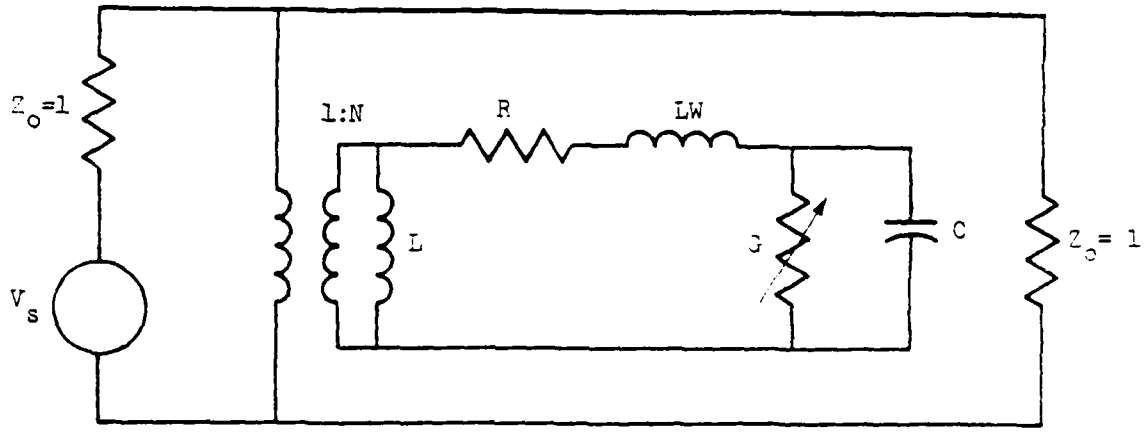


FIGURE 5 EQUIVALENT CIRCUIT WITH SERIES INDUCTANCE

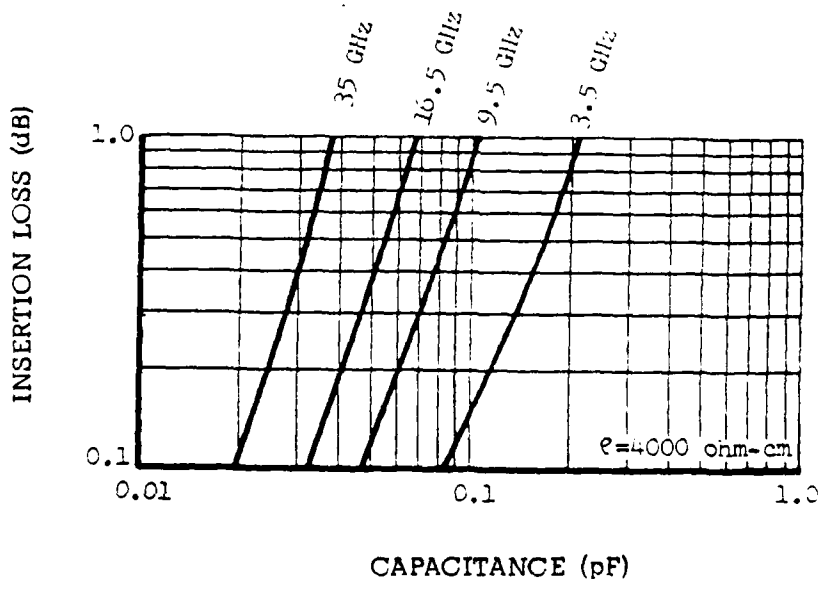


FIGURE 6 MID-BAND INSERTION LOSS vs CAPACITANCE AND FREQUENCY

The 3 dB bandwidth resulting from the circuit in Figure 5 is presented in Figure 7 as a function of capacitance and frequency. The midband insertion loss can be estimated from the dashed lines provided on the graph corresponding to 0.1, 0.4, and 1.0 dB loss.

5. High-Power Limiting

The limiting characteristic is defined by the graph of transmitted power (P_t) versus incident power (P_{in}). As discussed previously, the insertion loss (IL) is given by P_{in}/P_t and is dependent upon the limiter element conductivity (σ). At low levels σ is essentially constant having a value dependent upon the impurities in the semiconductor. At higher levels, the value of σ increases due to the impact ionization and the creation of electron-hole pairs which occur in the semiconductor at high electric fields. Both theoretical and empirical expressions relating σ and the average electrical field (E) were described in reference 1. An empirical relation is used in the present design work and is given below:

$$E(\sigma > 0.03) = \frac{\ln(\sigma + 0.00775) - \ln(0.008)}{1.035 \times 10^{-4}}$$

$$E(\sigma < 0.03) = \frac{\ln\sigma - \ln(0.00754)}{9.21 \times 10^{-5}} \qquad (5)$$

This relation was obtained using data from X-band components.

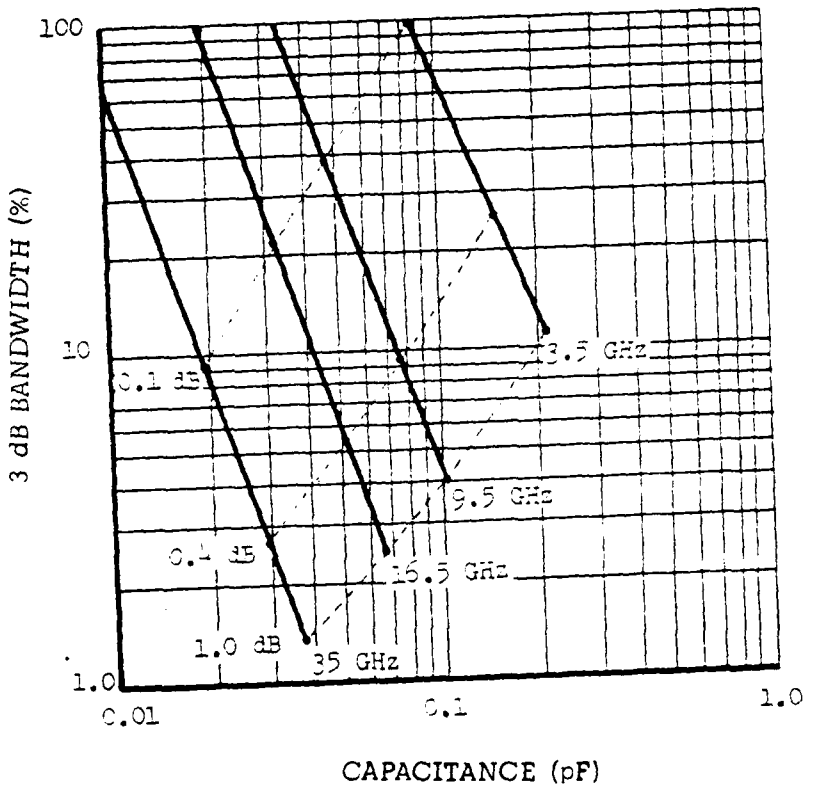


FIGURE 7 BANDWIDTH vs CAPACITANCE AND FREQUENCY

The transmitted power (P_t) is the transmission line voltage squared at the output port divided by the line impedence (Z_o). The transmitted voltage is conveniently obtained by transforming the limiter element voltage which is the limiter element thickness (W) times the average electric field (E), back to the transmission line by means of the circuit in Figure 5. Thus, by choosing values for σ, it is possible to calculate corresponding values for the insertion loss, and the input and output power levels. This data is presented in the limiting characteristics of Figures 8 and 9.

Before discussing these limiter design curves further, consider briefly the temperature within the limiter element. As the peak incident power is increased, the peak element temperature will increase. The temperature distribution and time factors were considered in detail in reference 2. It was indicated there that for the purpose of comparing element geometries a simple thermal capacitance model could be used for pulse lengths of around 1 μsec or less and low duty cycles. Peak temperatures are calculated for this model by means of Equation 6.

$$TEMP = 25 + \frac{P_{in}^2 \left(\frac{1}{\sqrt{IL}} - \frac{1}{IL} \right) tp\, \epsilon}{1.77\, Cs\, W^2} \qquad (6)$$

where

Temp	=	peak temperature at end of RF pulse (^oC)
tp	=	RF pulse length = 1 μsec
Cs	=	silicon capacitance (farads)
W	=	element thickness (cm)

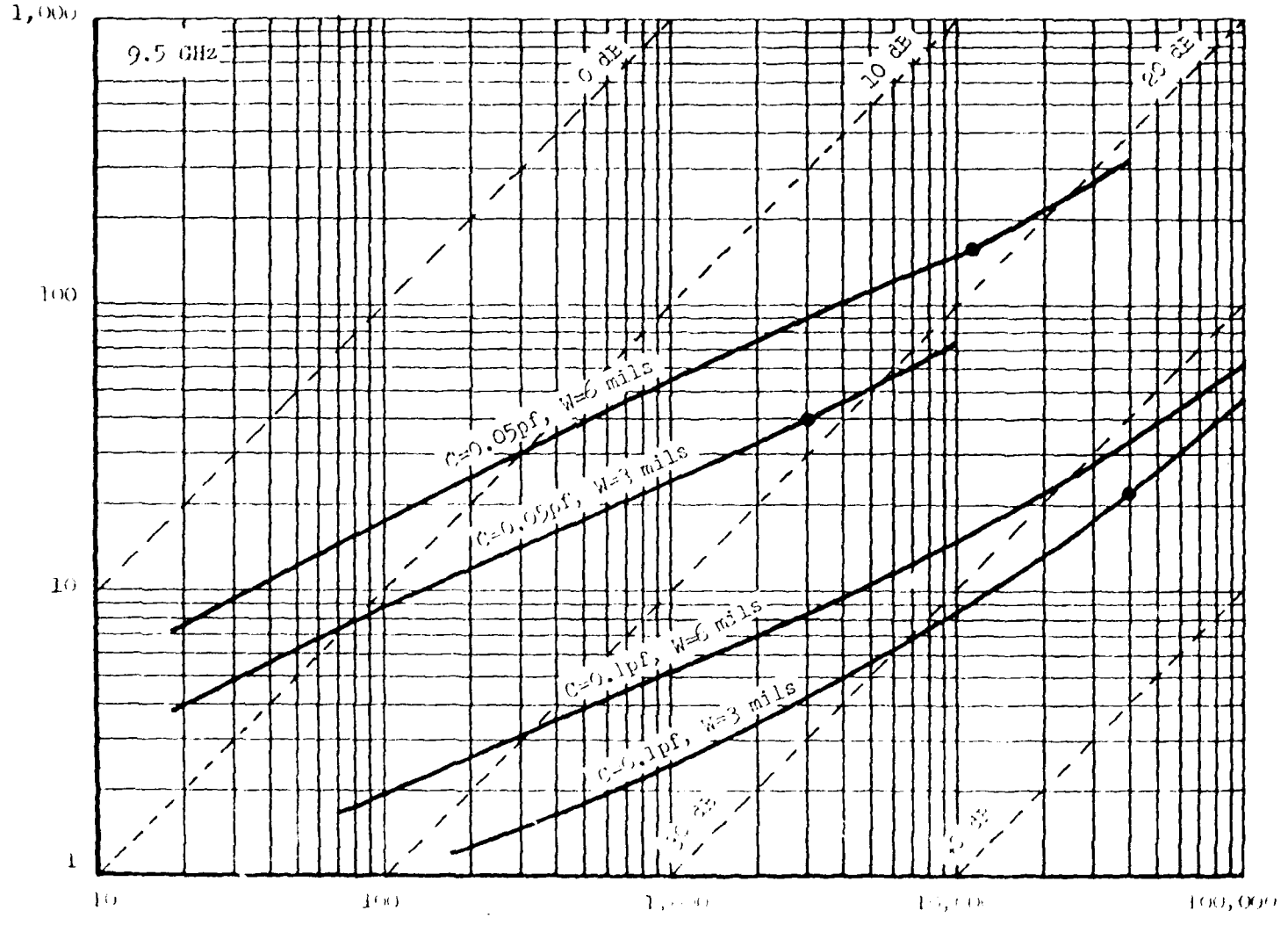


FIGURE 8. X-BAND LIMITER [illegible]

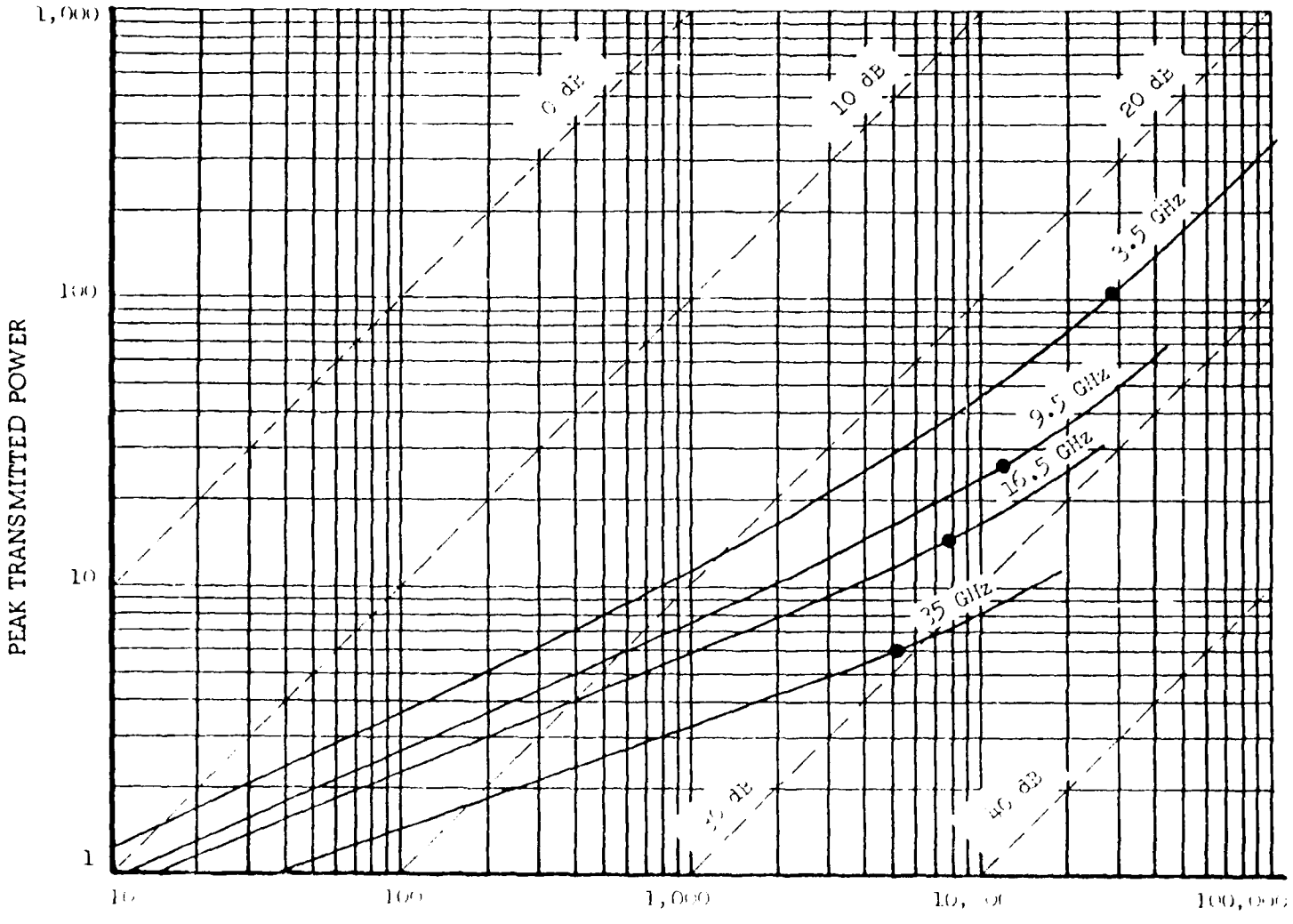


FIGURE 9 LIMITING PERFORMANCE AT OTHER FREQUENCIES

The limiter curves in Figures 8 and 9 are terminated at the power level where the peak temperature reaches 250°C. The large dot on the curves indicates a peak temperature of 125°C. Temperatures resulting from operation with pulse lengths other than 1 μsec will be different and can be calculated using Equation 6.

The design curves in Figure 8 portray the limiting performance to be expected at 9.5 GHz (X-band) by limiters using elements of two different thicknesses (3 and 6 mils). As expected, higher capacitance units provide higher isolation and power capability. For a given capacitance, elements twice as thick give approximately 3 dB less isolation and have about 4 times the power capability.

Notice also from the curves of Figure 8, the rather strong dependence of limiter performance on the element capacitance. Most of the X-band units built during the program have capacitance values in the 0.07 to 0.12 pF range and gave performance as indicated by the 9.5 GHz design curve of Figure 9 which is for 0.075 pF.

Double slit units with an element in each slit are electrically similar to a single slit, single element unit where the capacitance value is equivalent to the series combination of the two element capacitances and the one extra wire inductance (LW). The double slit experimental limiter provided performance in accordance with the 0.05 pF, 6 mil curve of Figure 8.

Notice in Figure 9 that useful limiting performance is projected for all of the frequencies presented. Although the low level loss is the same for these curves, the bandwidth is not (reference Figure 7).

In summary, this section has provided data and curves relating the physical element parameters to the limiting performance expected. This information is useful both in assessing operation in new applications and also in providing the actual fabrication design data.

D. Circuit Analysis of the Bulk Limiter

1. Introduction

The bulk semiconductor limiter element is a high impedance microwave device which has an electrical conductivity which is a function of the microwave voltage across the device. The circuit with which the element is used must meet certain requirements to yield optimum low and high power microwave performance. For example, incident low level microwave power absorbed by the device contributes to insertion loss. The percentage of low level power absorbed by the device can be easily reduced by lowering the circuit impedance at the limiter element terminals. Note that for any given limiter element that lowering circuit impedance would also widen the bandwidth substantially as the capacitive susceptance of the limiter element would have a smaller effect in the lower impedance circuit.(*) Thus, lowering the circuit impedance presented across the limiter element terminals improves the low level characteristics of the completed component.

An examination of the high power isolation state of the limiter device shows the lowering the circuit impedance at the element terminals reduces the isolation which results from a given element conductance. The reduction in isolation results in an increase in dissipated power within the device and consequently reduced power handling capability and increased return loss. Thus, lowering the impedance at the element terminals degrades all high power performance characteristics.

As a consequence, it is necessary to select the transmission line impedance presented to the limiter element terminals at a compromise value which provides both optimum high level and low level performance. Further, in designing tuning circuits to provide for broadband

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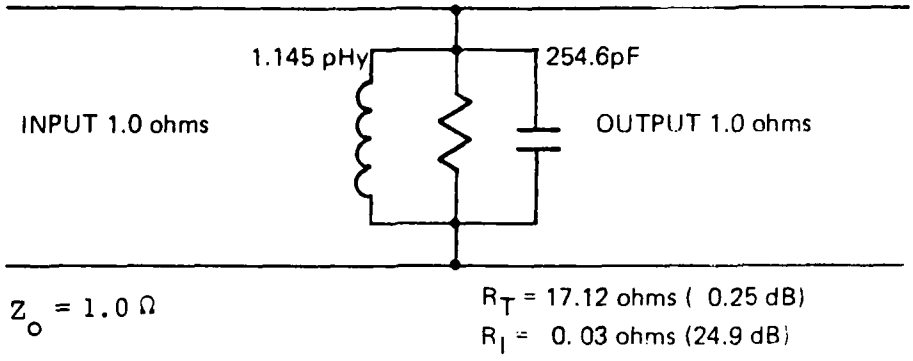
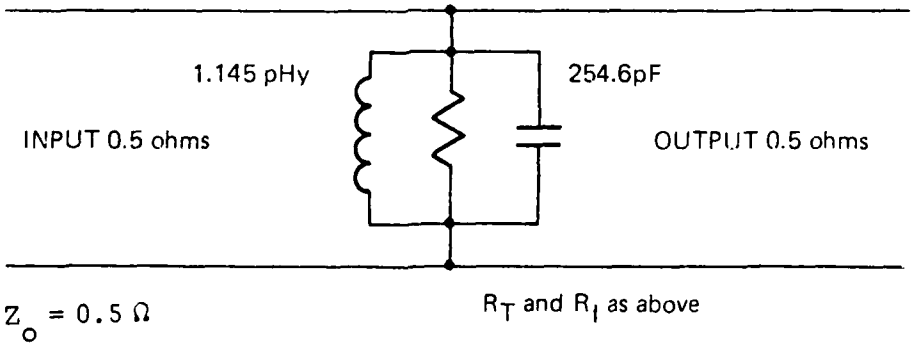
NOTE* ECOM-0292F - Bulk Semiconductor limiter DAAB07-72-C-0292 PP 23 - 36.



(a) NORMALIZED TO 1.0 OHM



(b) IN REDUCED IMPEDANCE LINE

FIGURE 10 BULK LIMITER EQUIVALENT CIRCUIT

D-15463

low level characteristics, it must be remembered that high power performance will be affected by the choice of that design. For optimum performance over the band of operation, a frequency independent impedance at the element terminals is desired.

2. Example

To illustrate the effects of the impedance at the plane of the limiter element, consider the case of the bulk limiter design shown in Figure 10(a). The design has been simplified by eliminating the turns ratio and transforming the reactance values to a normalized 1 ohm transmission line.

Let us consider the following experimental parameters under low and high power conditions of the circuit in Figure 10 (a).

- Circuit [10a] Low Power

  f_o = 9.32 GHz

  BW (3 dB) = 1.25 GHz

  IL = 0.25 dB

- Circuit [10a] High Power

  Isolation = 24.9 dB

  Fractional Power Dissipated $\frac{P_d}{P_i}$ = 0.107

The relationships: (for details see Reference 11)

$$\frac{P_i}{P_t} = \left| 1 + \frac{Y Z_o}{2} \right|^2$$

and

$$\frac{P_d}{P_i} = \left| \frac{Z_o G}{1 + \frac{Y Z_o}{2}} \right|^2$$

are used to calculate R_T parameters.

R_T (Low-Power) = 17.12 Ω and R_T (high-power) = 0.03 ohm*

Now, assume that the transmission line has a lower impedance in the plane of the limiter element caused by the matching circuitry used. The impedance of the circuit shown in Figure 10(b) is reduced by a factor of two to a value of 0.5 ohm. Again, calculating the low and high power performance of the limiter circuit yields:

- Circuit [10b] Low Power (R_T = 17.12 ohms)

  f_o = 9.32 GHz

  BW (3 dB) = 2.5 GHz

  Calculated Insertion Loss = 0.13 dB*

- Circuit [10b] High Power (R_I = 0.03 ohm)

  Calculated Isolation = 19.4 dB*

  Calculated Fractional Power Dissipated $\frac{P_d}{P_i}$ = 0.191*

* For details see Appendix IV.

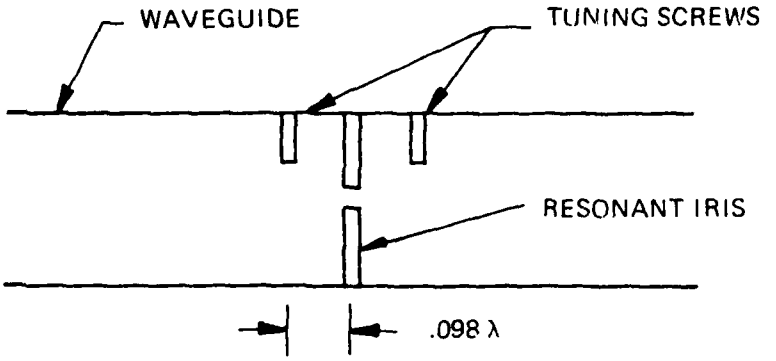
Thus, while the circuit of Figure 1(b) improved low power performance greatly by minimizing the insertion loss and broadening the bandwidth of the device, it did so only at the expense of high power performance. The isolation was reduced from 24.9 dB to 19.4 dB and the power absorbed by the device from the incident microwave pulse increased by a factor of 1.79. Thus, the power handling capability of the device was reduced by a similar factor.

The above example was given to illustrate that the impedance presented by the circuit to the limiter element terminals is extremely important in its effects on device operation and power handling capability. A bulk limiter element will be capable of dissipating a fixed amount of energy during a high power microwave pulse. Therefore, in order to maintain both good high and low power performance characteristics, the matching circuitry used to couple the bulk semiconductor state to the lower power stages must be well understood.

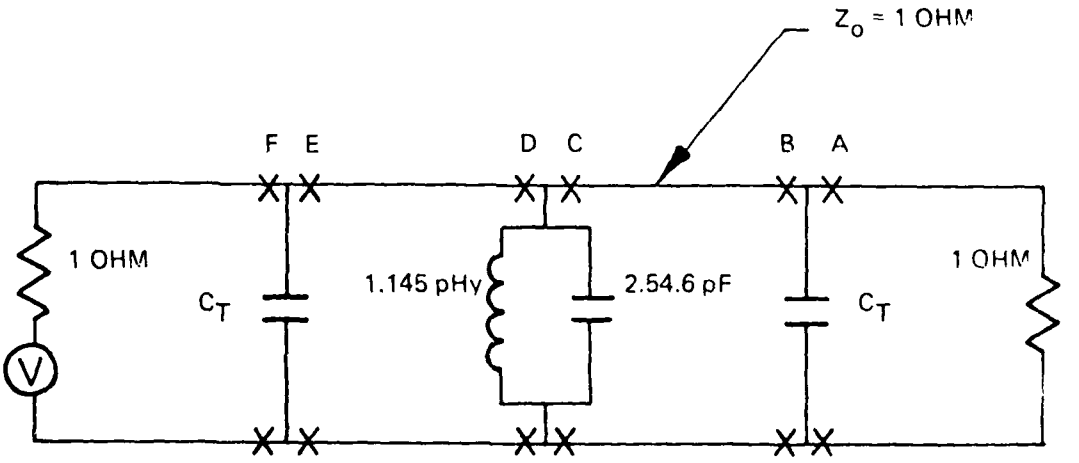
3. Capacitive Tuning

Now examine the effect of using symmetrical capacitive tuning arrangement on either side of the bulk limiter. Figure 11(a) shows the geometrical arrangement of tuning screws which will successfully match present bulk limiters to the low level PIN stages at low power levels. Figure 11(b)is an equivalent circuit of the above structure with the waveguide impedance and limiter element values normalized to 1 ohm. C_T represents the capacitance of the tuning screws in the transmission line.

The object is to match the power from the one ohm input port to the load resistor over the frequency band of interest. For the sake of simplicity, we can analyze the transmission state with $R = \infty$, the lossless case. From the transmission line theory, it is known that if one



(a) PHYSICAL CIRCUIT



(b) EQUIVALENT CIRCUIT

FIGURE 11 CAPACITIVE TUNED BULK LIMITER

divides the transmission line at any point, the impedance of the portion looking toward the source must equal the complex conjugate of the impedance of the portion looking toward the load for maximum power transfer to occur. Thus, if a matched transmission line circuit were cut and the impedance of the load portion were measured at

$$Z_L = 0.7 + j\,0.5 \text{ ohm}$$

then it follows that the impedance of the source portion would be

$$Z_S = 0.7 - j\,0.5 \text{ ohm} .$$

Similarly, if a symmetric circuit were divided at the center, it follows that for a matched condition to exist the impedance of both halves would necessarily be real and equal.

This leads to the analysis of the circuit of Figure 11(b) at 9.32 GHz. The Smith chart of Figure 12 shows the impedance of the circuit calculated from the load end. Assume a susceptance value of +j 0.7 has been used for C_T. Point A is the impedance of the 1 ohm load and transmission line. Point B includes the susceptance of the load side capacitor C_T. At Point B, the impedance of the cirt looking toward the load is $Z_B = 0.67 - j\,0.47$ ohm. As we move back toward the generator by approximately 1/10 wavelength, Point C, we find the impedance to be entirely real with a value of 0.5 ohm. At resonance, 9.32 GHz, the limiter circuit appears as an open circuit (lossless case) and the impedance at Point D is the same as that at Point C. Moving back another 1/10 wavelength yields a load impedance from Point E of $Z_E = 0.67 + j\,0.47$. This inductive component is cancelled out by the generator side susceptance

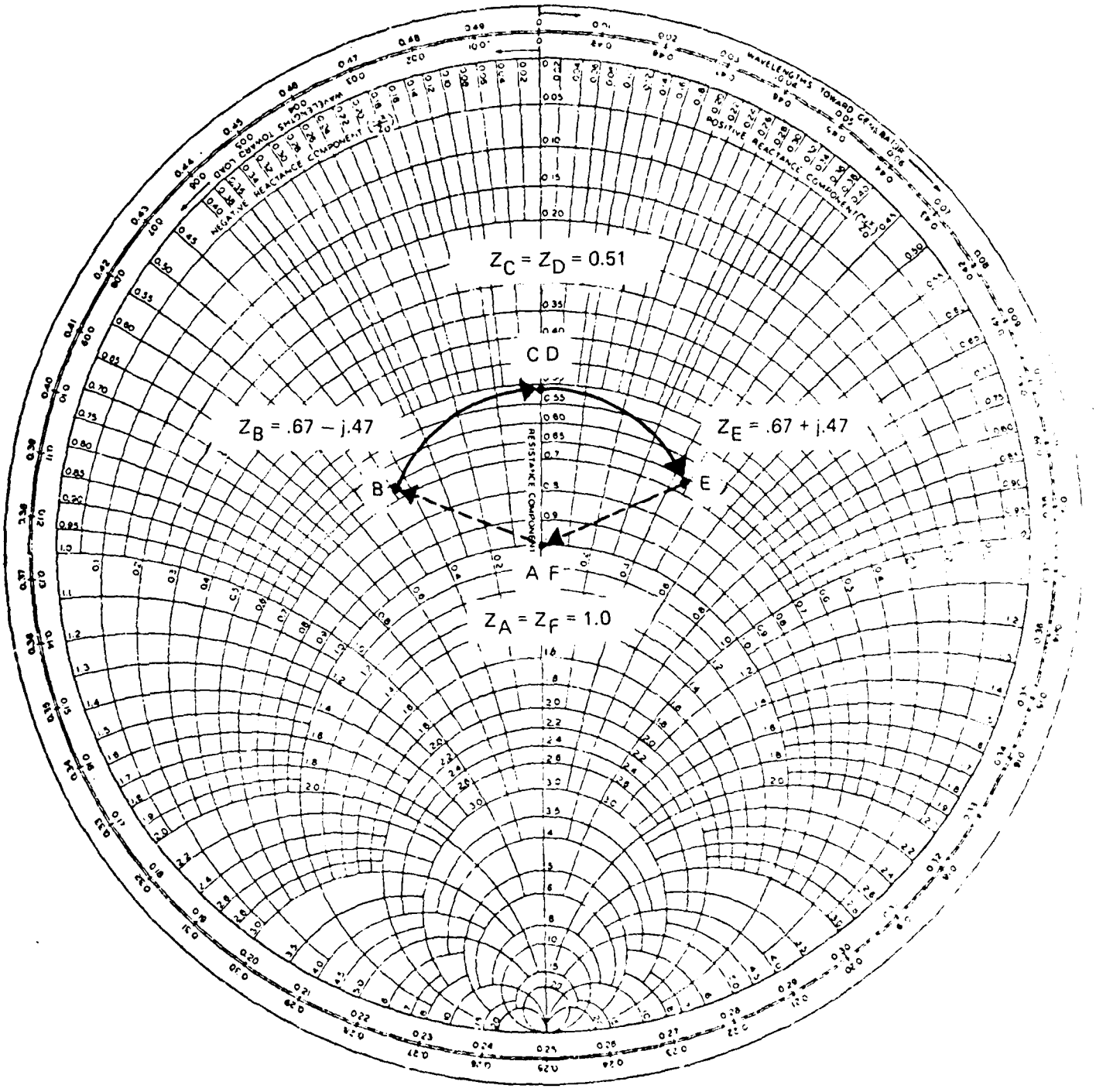


FIGURE 12 IMPEDANCE PLANE ANALYSIS OF CAPACITIVE TUNED BULK LIMITER

of C_T = j 0.7 mhos yielding a load side impedance of 1.0 ohms at Point F. Analysis of the same circuit at the band edges of 9.0 and 9.65 GHz yields the following results:

Without Tuning:

f_o	S_{11}	IL
9.0 GHz	0.46 <) -63 °	1.04 dB
9.32 GHz	0 <) 0 °	0.0 dB
9.65 GHz	0.46 <) +63 °	1.04 dB

With Tuning Capacitors spaced 0.098 λ at 9.32 GHz, B = 0.7 mhos @ 9.32 GHz

f_o	S_{11}	IL
9.06 GHz	0.24 <) 179°	0.26 dB
9.32 GHz	0 <) 0°	0.0 dB
9.65 GHz	0.22 <) -38 °	0.21 dB

In performing the analyses, the following impedances were noted as a function of frequency at the iris plane [Point C in Figure 11(a)]:

Frequency	Admittance	Impedance
9.0 GHz	1.91 + j 0.06	0.523 - j 0.016
9.32 GHz	1.98 + j 0	0.505 + j 0
9.65 GHz	2.03 - j 0.1	0.491 + j 0.012

Thus, it is seen that the effect of the two tuning capacitors of Figure 11(a) is primarily to lower the circuit impedance at the plane of the resonant limiter iris. Very little reactive tuning occurs because the capacitors do not present a rapidly varying susceptance at the window plane.

4. Circuits for Consideration

It has been shown that waveguide tuning circuits which do not present rapidly varying reactance at the limiter element plane can only improve low level performance by reducing the resistive impedance component at the limiter element plane. This deteriorates the high level performance severely. Hence, only circuits with long spacial dimensions or rapidly varying reactance versus frequency characteristics will be capable of providing the desired performance (see Figure 13).

Circuits capable of providing the desired performance are shown in Figure 14. Both circuits will show a mid-band frequency shift either upward (for spacings of approximately 0.17 λ) or downward (for spacings of approximately 0.33 λ). One of these two circuits or a variation thereof will have to be used for achieving broadband performance from the bulk limiter in a short length of waveguide.

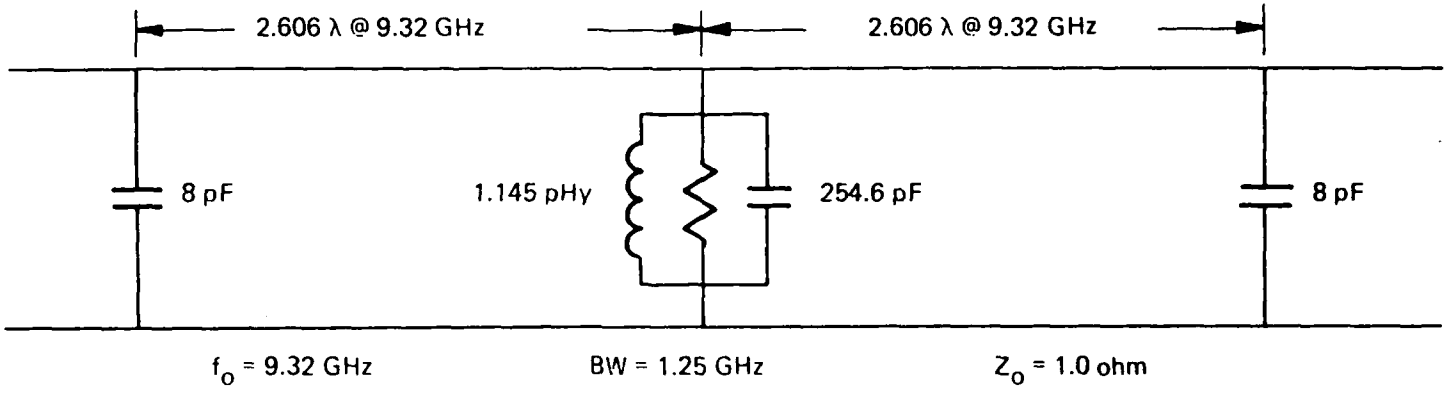


FIGURE 13 BULK LIMITER BROADBAND TUNED WITH WIDE SPACED CAPACITORS

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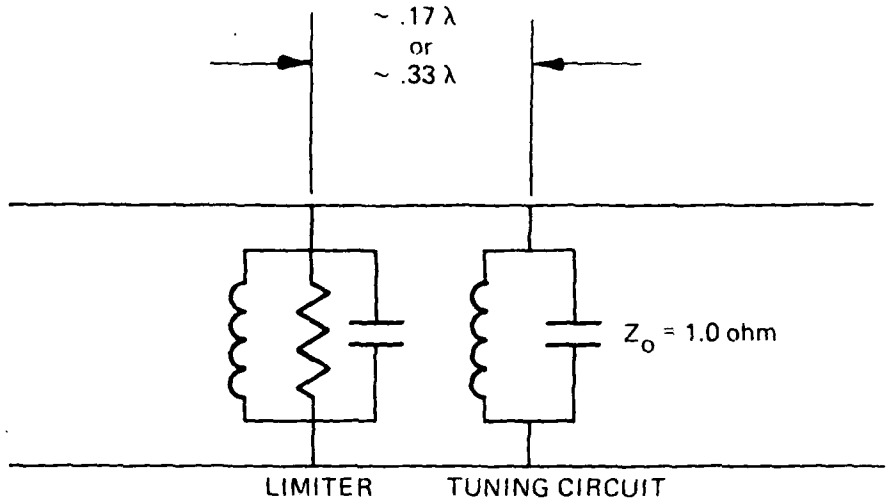
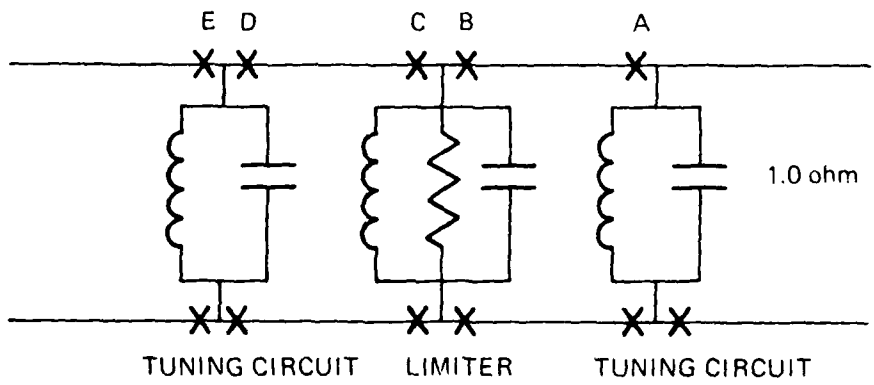


(a) SINGLE TUNING CIRCUIT DESIGN



(b) DOUBLE TUNING CIRCUIT DESIGN

FIGURE 14 RESONANT CIRCUIT BROADBAND TUNING OF BULK SEMICONDUCTOR LIMITERS

Analysis of the two circuits shown in Figure 14 produces the conclusion that circuit 14(b), the double tuning circuit, will provide the best limiting performance. Figure 15 shows a complete analysis of circuit 14(b) using the following circuit parameters:

- Limiter Iris Parameters

  f_o = 9.15 GHz

  BW (3 dB) = 1.25 GHz

  R = ∞ (lossless case)

  C = 254.6 pF

  L = 1.88 pHy

- Tuning Iris Parameters

  f_o = 9.15 GHz

  BW (3 dB) = 2.50 GHz

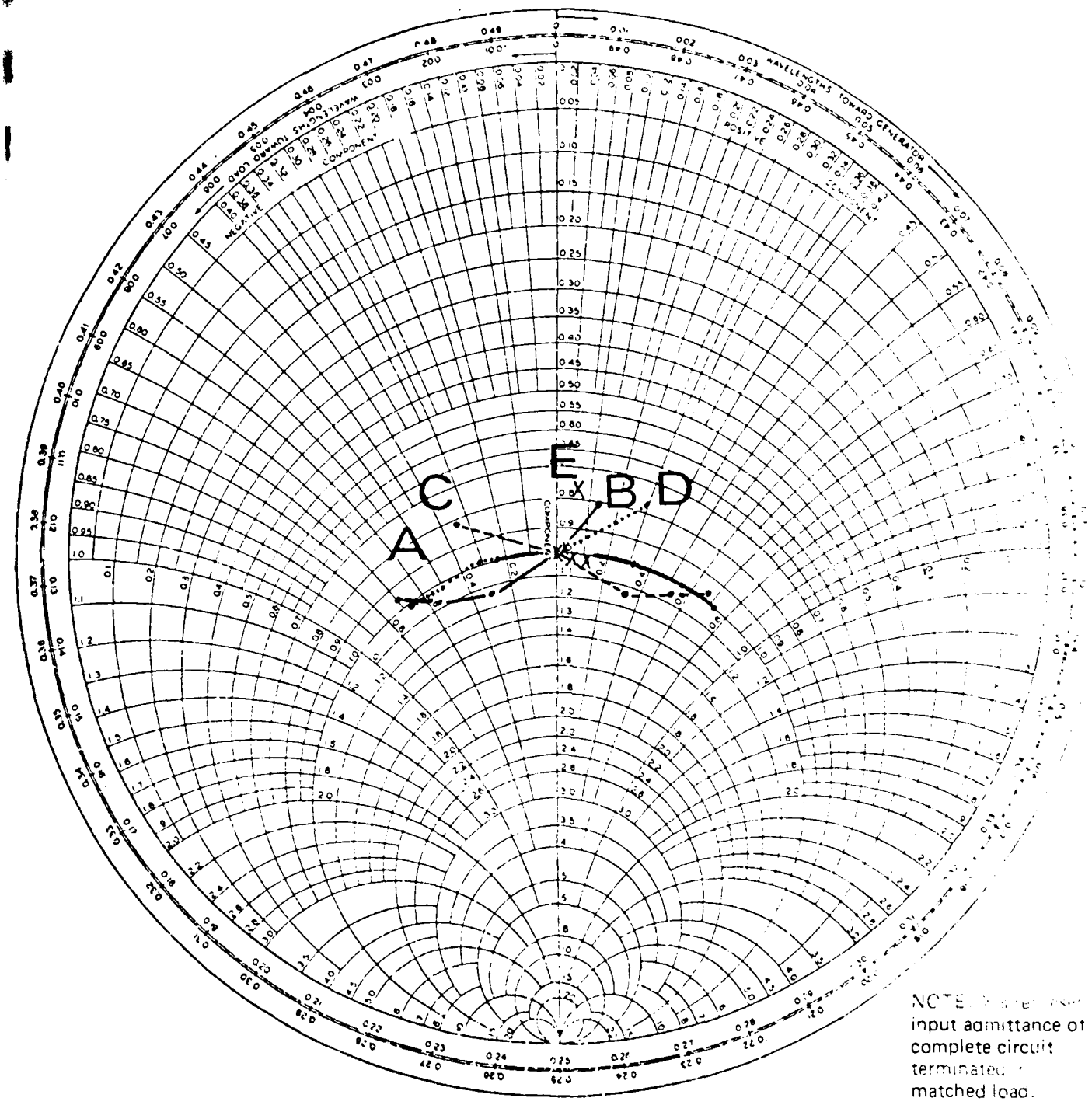
  C = 127.3 pF

  L = 2.376 pHy

- Tuning Iris to Limiter Spacing

  Spacing = 0.191 λ at 9.15 GHz

The analysis was carried out at five frequencies within the operating bandwidth 9.0, 9.15, 9.35, 9.5, and 9.65 GHz. The curves on the admittance plane plot (Figure 15) represent the various lettered points on the circuit diagram [Figure 14(b)] as a function of frequency. All curves are labeled at their low frequency end and the 9.15 GHz point on all curves is coincident with the origin. The input admittance to the circuit (Plane E admittance) is shown by points labeled X on the Smith chart.



NOTE: Point E is the input admittance of complete circuit terminated in matched load.

FIGURE 15 ADMITTANCE PLANE ANALYSIS OF CIRCUIT 5b

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It is important to note two factors in this analysis. First, very good matching was obtained over the 9.0 GHz to 9.65 GHz frequency range of interest. The magnitude of S_{11} is less than 0.14 for all frequencies. This corresponds to a return loss of greater than 17 dB which more than meets the VSWR specification of 1.4:1. Second, the impedance at the limiter element plane does not vary too much with frequency. This can be seen by reading the conductance value off of either curve B or C as a function of frequency. Minimum conductance is 0.78 mhos; maximum is about 1.13 mhos. Thus, the impedance variation is 1.45 to 1. Careful examination of the Smith chart shows that this can be reduced still further by a slightly wider spacing of the tuning elements.

5. Recommended Circuit Configuration for a Multi-Stage Limiter

It is recommended that the left portion of the circuit, Figure 14(b), be the tuning design for the multi-stage limiter component; thus, the circuit should consist of:

(a) An input pressure window resonant at 9.1 - 9.15 GHz, with a bandwidth of twice the limiter bandwidth.

(b) A section of waveguide transmission line approximately 0.19 wavelengths long at the iris f_o.

(c) The bulk limiter stage (minimum bandwidth approximately 1.35 GHz).

The remaining reactive tuning, supplied at Plane A in Figure 14(b) can be supplied by the low level limiter stage provided that the spacing between the bulk limiter and the low level stage has the proper value.

It is very important to note that as long as the circuit to the left of the bulk limiter contains only those components and

spacings specified, no tuning element placed on the right of the bulk limiter will affect power handling capability adversely. Thus, tuning screws and the like can be used as desired to obtain low frequency performance.

6. Test of Three-Stage Filter Design

A three-stage filter design was analyzed at RRC for achieving the necessary tuning. The bulk limiter stage was assumed to have the following characteristics of frequency and bandwidth:

$$f_o = 9.15 \text{ GHz}$$

$$\text{BW (3 dB)} = 1.25 \text{ GHz}$$

These values were based, in part, on the results of the first engineering samples. The 1.25 GHz bandwidth should be obtainable simultaneously with a 30 kW power capability if two bulk limiter elements are used in either a double or single slot iris.

Two passive irises with the same center frequency, 9.15 GHz, and twice the 3 dB bandwidth or 2.5 GHz, were used in the design. The completed filter structure has a passive tuning iris, the active bulk semiconductor limiter, and a second passive tuning iris all separated by 0.19 wavelength spaces. The theoretical analysis indicated a bandwidth considerably in excess of the needed 650 MHz. Further, the analysis showed minimal impedance variation of the limiter plane as a function of frequency. Hence, good performance was anticipated.

Unfortunately, in high power testing the circuit, it was found that the electric field across the input tuning iris was very high and arcing occurred during high power testing. Thus, without development of a tuning resonator capable of withstanding the high power pulses without arcing, this circuit cannot be used.

In order to evaluate the effectiveness of the three-stage tuning mechanism, a test was run at RRC to optimize the structure for input VSWR. The test included a two-stage diode limiter similar to MA3940X as part of the structure. No tuning screws were used to optimize the structure, as tuning screws in front of the bulk limier will reduce the impedance at the limiter. The overall mechanical arrangement is as shown in Figure 16, as are the parameters of the three resonant irises used in the experiment. The result of the test was a return loss of 16 dB or greater over the frequency range of 9.080 to 9.805 GHz or a 1.38:1 VSWR over a 725 MHz bandwidth. The insertion loss varied from 0.9 dB at the bottom of the passband to 0.7 dB over the rest of the operating bandwidth.

Thus, the three-stage filter in front of the diode limiter is capable of providing the necessary tuning. However, we cannot implement it without first coming up with a tuning iris that can withstand the high fields caused by the reflected power under high power conditions.

7. Alternate Filter Design

Thus, it is necessary to examine filter structures which do not require an input filter element in front of the bulk semiconductor limiter. The bulk semiconductor limiter becomes conductive under high power conditions. Therefore, it does not arc because the electric field is greatly reduced by the shunt conductance at the iris plane. Tuning elements located on the low power side of the bulk limiter are never exposed to high values of electric field because of the shorting action of the bulk limiter. Therefore, any design which utilizes the bulk limiter itself as the input stage will not require high power tuning elements. It should also be noted that no impedance transformation can occur if the bulk limiter is the input stage of the filter structure. Thus, the

IRIS PARAMETERS

IRIS	f_o	BW (3 dB)	IL
B3	9.28 GHz	1.21 GHz	0.25 dB
B5	9.30	2.44	0.05
B6	9.30	2.37	0.05

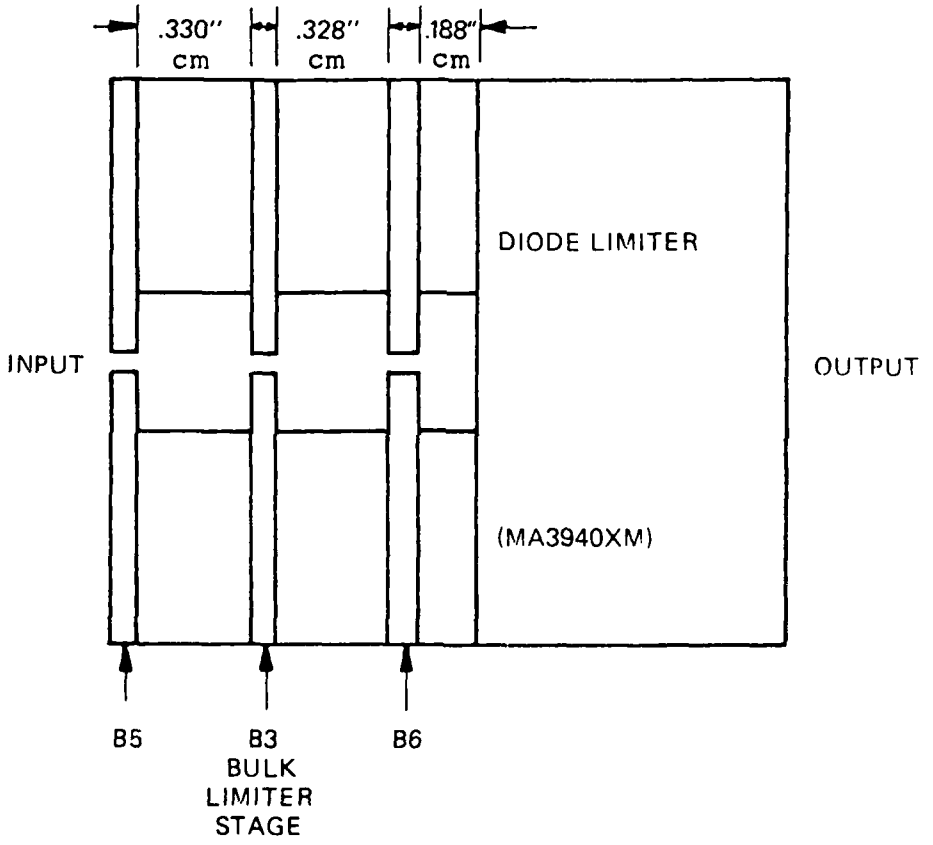

FIGURE 16 THREE STAGE FILTER TEST

power handling, insertion loss and recovery characteristics of the bulk limiter should be essentially independent of frequency.

An analysis of a simple two element filter using identical resonant irises spaced apart by a section of waveguide was performed. Based on geometrical Smith chart observations, two spacings were examined, 0.25 wavelengths and 0.186 wavelengths. The conclusion was reached that using lossless resonant irises with resonant frequencies of 9.15 GHz and 3 dB bandwidths of 1.25 GHz, the maximum 1.4:1 VSWR bandwidth occurs at a spacing of 0.186 wavelength and is approximately 445 MHz. This result did not include possible tuning effects of the diode limiter stage which were difficult to incorporate in the analysis. It was, therefore, decided to conduct a set of experimental tests to evaluate the performance to be expected.

8. Limiter Input Filter Results

Considerable experimentation was performed with the bulk limiter state (a dummy iris with known center frequency, bandwidth, and insertion loss) as the input stage of the filter. The best result was obtained with the tuning structure including the MA3940XM diode limiter stage shown in Figure 8. The diode limiter was adjusted to provide the maximum 1.4:1 VSWR bandwidth as was the tuning screw shown in the Figure. The best result obtained was a passband from 9.045 GHz to 9.634 GHz or a 589 MHz bandwidth. This is slightly less than the 650 MHz desired, but indicates that the circuit is nonetheless usable. It is anticipated that adequate performance could be relaized if the bandwidths of irises B4 and B3 were greater by 15 to 20%.

It is, therefore, concluded from the experimental results of the low power filter testing that a limiter input filter as shown

IRIS PARAMETERS

IRIS	f_o (GHz)	BW (3 dB) (GHz)	IE (dB)
B4	9.29	1.15	0.20
B3	9.28	1.21	0.25

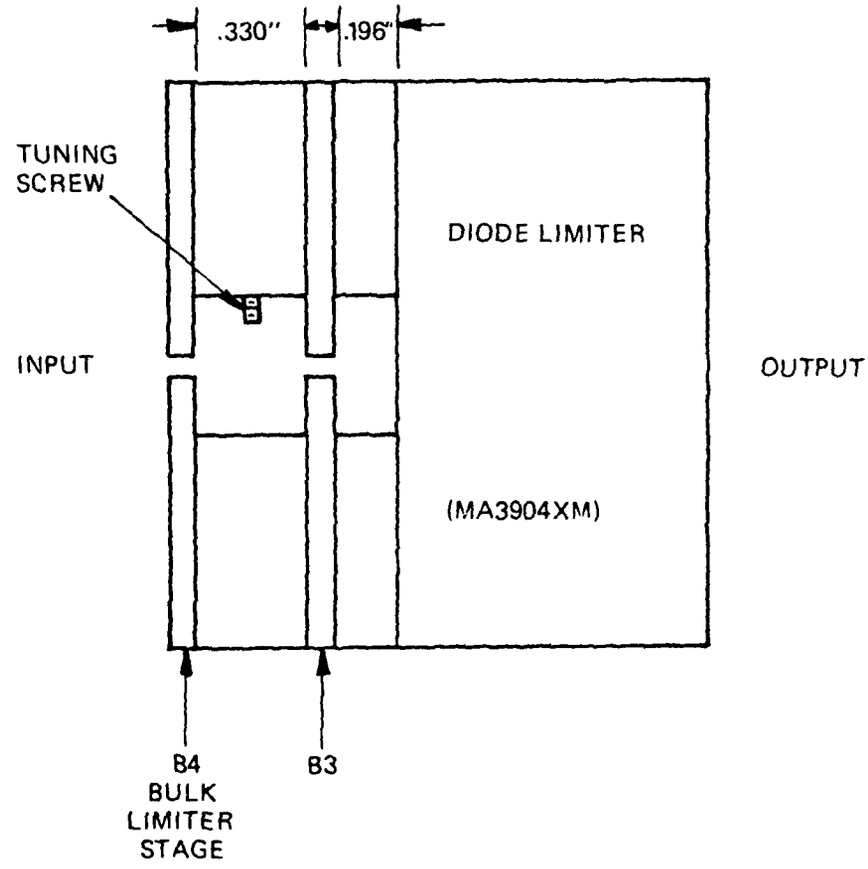

FIGURE 17 TWO STAGE FILTER EXPERIMENTAL TEST

in Figure17 will yield the desired 650 MHz passband provided that the 3 dB bandwidth of the high power limiter stage is 1.32 GHz or greater. It should be understood that any tuning mechanism used on the low power side of the bulk limiter will neither be required to withstand high levels of mmicrowave power nor reduce the impedance at the limiter plane at any frequency. Hence, the power capability of the bulk stage will not be affected by the tuning or low level stage.

It is also worth noting that the diode clean-up limiter does not have the optimum reactive tuning characteristics to broadband the two-stage bulk semiconductor limiter. It is a wide bandwidth structure designed to have a flat passband. Therefore, it cannot present a matching reactance to the bulk limiter tuning iris circuit in the middle of the operating bandwidth.

Observations of the tuning interaction between the bulk limiter tuning iris stage and the diode limiter stage indicate that the reactance of the diode limiter stage interacts with that of the bulk limiter stage at one of the two-band edges. The spacing of the bulk limiter and tuning iris must be such that the VSWR does not exceed the 1.4:1 specification at the filter's center frequency when tested along. The parameters of the diode limiter can then be adjusted in the assembled package to broaden the passband on either the low or high frequency end. The return loss characteristic observed for the tuned structure of Figure 17is shown in Figure 18. There are three mimima in the return loss characteristic within the 589 MHz bandwidth defined by the 1.4:1 return loss specification.

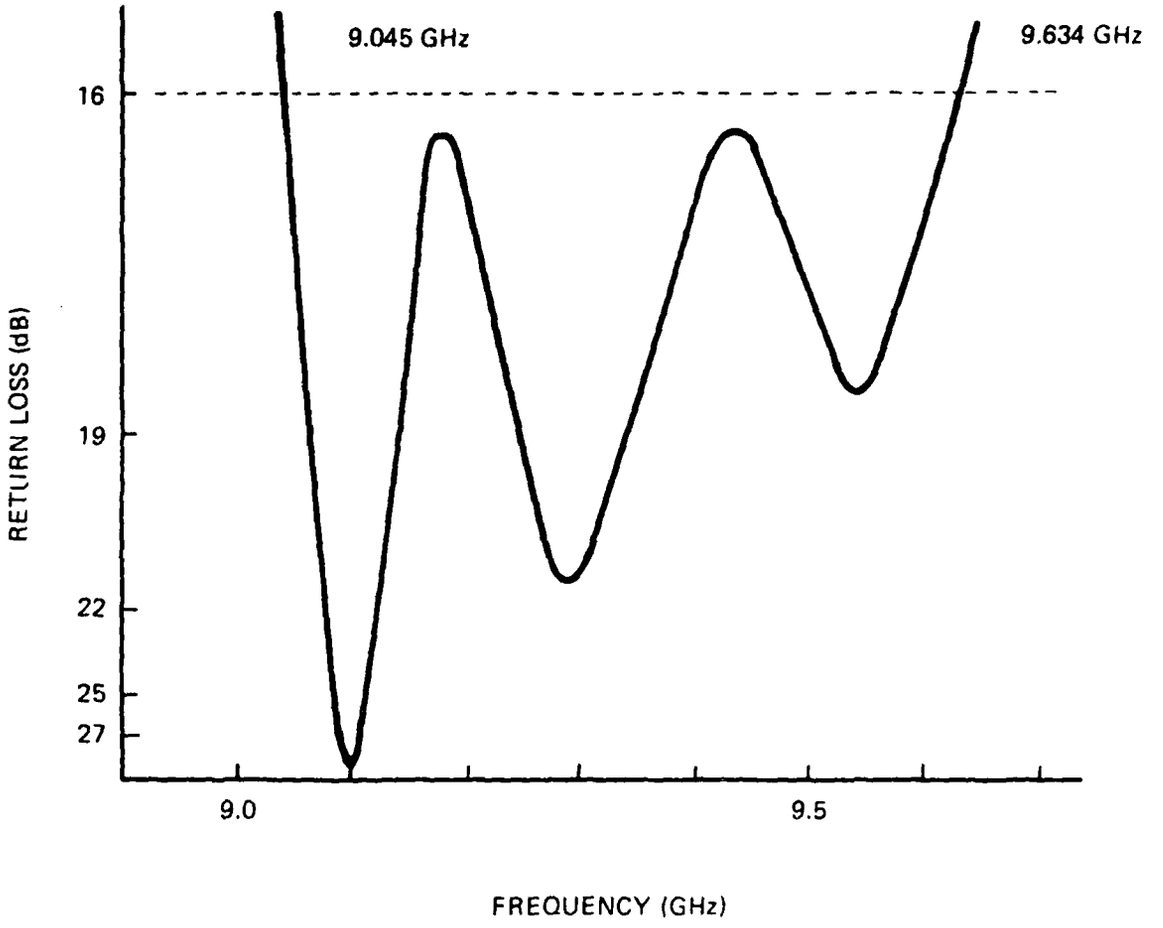

FIGURE 18 RETURN LOSS CHARACTERISTIC OF LIMITER INPUT FILTER

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E. Design Improvements and Final Design of the Bulk Semiconductor Limiter

During the engineering phase, significant improvements in the fabrication procedures of bulk limiters were accomplished. A batch fabrication scheme was introduced to improve the manufacturability of bulk limiters. The delicate diffusion bonding of the bulk limiter chip[5] 10 mil gold wire was replaced by ball bonding the gold wire to a 3 mil etched gold post defining the active area.[9] A high eutectic temperature metallization scheme, consisting of titanium-tungsten (10% Ti and 90% W) and gold was introduced to improve the power handling of bulk limiters.[9]

F. Fabrication of Bulk Limiters

1. High Resistivity Silicon Material

The quality of high resistivity uncompensated silicon material is probably the most important requirement for manufacturing high power and low insertion loss semiconductor bulk limiters. Very high resistivity uncompensated silicon cannot be grown by epitaxial processes. Thus, the use of epitaxial wafers in bulk limiter fabrication is ruled out and all processing must be accomplished using very thin float-zone refines silicon wafers. The important parameters that one must control are low crystalline defect density, controllable doping density, and precisely controllable wafer processing steps.[8,9]

2. Wafer Dicing and Polishing

High resistivity silicon ingot was used to fabricate the bulk limiters. The ingot was grown by the float-zone method by Wacker Chemical Company, Munich, West Germany. It is ingot number W30736-6, resistivity 10.4 - 15.0 x 10^3 ohm/cm, ⟨111⟩ orientation, p-type, uncompensated with lifetime of 2 x 10^3 microseconds.

The ingot was mounted on a graphite block with epoxy resin. The wafers were then saw cut 10 mils thick on the ⟨111⟩ orientation on an STC (Silicon Technology Corporation, Oakland, New Jersey) inside diameter slicing machine. At this point in the as-sawn condition, maximum linear thickness variation was less than 0.4 mil and maximum bow was approximately less than 0.2 mils.

The wafers were then chemically etched to remove at least one mil of silicon from each side. An etching solution of modified 6:1:1 (HNO_3:HF:HAc) mixture was used, resulting wafers varying in thickness from 7.8 to 8.4 mils.

These wafers were separated in 0.1 mil thickness increments and mounted on stainless steel polishing blocks. One side was chemically-mechanically polished; the wafers were dismounted and solvent cleaned, then remounted for opposite side polishing. Optimum process conditions of slurry pH, hydraulic pressure, slurry temperature, and polishing time were utilized. A final double-sided wafer polishing thickness for two separate processing runs of 3.5 - 3.6 mils and 3.8 - 4.2 mils respectively, were obtained. Linear thickness variation of 0.2 mil maximum was obtained.

It appears that appropriate processing conditions for slicing, etching, cleaning, mounting, and polishing have been developed to obtain damage-free, very high resistivity, very thin silicon wafers. Further, efforts were made to establish the reproducibility of these processing parameters. This method produced a flatter wafer, without sharp edges which permitted fabrication processes to proceed with lower breakage and consequently, improved yield.

3. Wafer Processing

First, silicon wafers were thinned down to 3.0 mil thickness by polishing and etching techniques. Then, the wafers were phosphorous diffused at 1000°C for 30 minutes (see Table III) using $POCl_3$ diffusion system. After the completion of phosphorous diffusion, the phosphorous doped glass on the wafer was etched in hydrofluoric acid and 1000 Å of a silicon diozide (SiO_2) glass was thermally grown at 1000°C.[9]

Both surfaces of the wafer were then photoprocessed in sequential operations which transfer the 0.75 mil checkerboard pattern of the photoresist mask to the silicon wafer. The checkerboard pattern windows were then etched through the SiO_2 and phosphorous doped silicon layers by using buffered hydrofluoric acid and 12:1:1 (HNO_3:HF:CH_3:COOH) respectively. The wafer was then diffused with boron at 950°C for 20 minutes using a boron nitride source. The boron diffused wafer was etched in hydrofluoric acid to remove all glass from the wafer surfaces.

Both surfaces of a wafer were then metallized with 500 Å layer of titanium-tungsten alloy (10% Ti, 90% W) and a 2000 - 3000 Å layer of gold and then electroplated with pure gold.[9] One surface was plated to a thickness of 0.1 mil while the other was plated to a thickness of 4.0 mils. Then bulk limiter wafers were saw-cut into 40 mil squares and were separated into individual chips. (See Tables I & II).

After diffusion bonding with 8 mil diameter gold wire, the chips were mesa etched in silicon etch and passivated with silicon nitride and Dow Corning DC-643 junction coating.[9] The bulk limiter chips were mounted in copper X-band irises and were tested for both low and high level RF performance.

4. Bulk Limiter Tuning

The bulk diode limiter assembly consists of the bulk limiter followed by a two-stage diode clean-up limiter. In combining the bulk limiter with the diode limiter, as shown in Figure 10, it was necessary to use tuning screws in front and back of the bulk limiter to achieve optimal bandwidth performance.[8] But this had an adverse effect on the peak power handling capability of the bulk diode limiter assembly. The peak power handling capability was reduced approximately by a factor of two. A matching structure was introduced in which all the tuning was accomplished with elements between the bulk limiter and clean-up limiter. A typical single-slot bulk limiter and its low level RF performance is shown in Figure 19 and Figure 20.

A dual-slot bulk limiter was also introduced[9] as shown in Figure 21 and Figure 22. A dual-slot bulk limiter exhibits wider bandwidth (see Figure 22) as predicted by the circuit analysis; but a dual-slot bulk limiter approach was found to be very expensive and time consuming. Besides selecting two bulk limiter chips completely matched, the failure mechanism of dual-slot bulk limiters cannot easily be predicted. A problem was encountered in predicting burnout of (one or two bulk limiters) dual-slot bulk limiters from recovery time measurements. Typically, single-slot units do not burnout until recovery time exceeds 2 microseconds. No pre-burnout indication was found with dual-slot units.

G. Fabrication of the Bulk-Diode Limiter Assembly

The bulk-diode limiter assembly consists of the bulk limiter followed by a two-stage diode clean-up limiter (as shown in Figures 23 through 26).[8] In addition, tuning screws are used to achieve broadband performance. (See Table II).

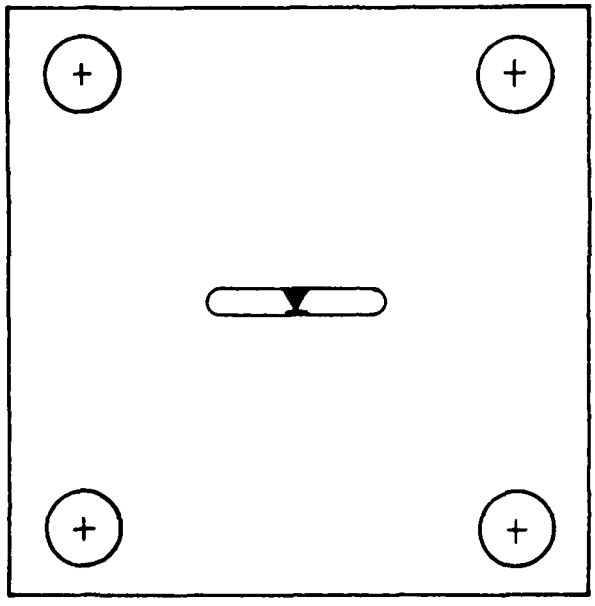
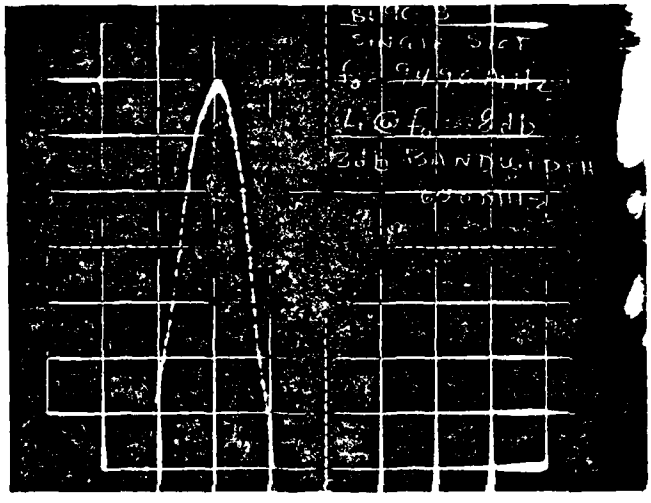


FIGURE 19 SINGLE SLOT BULK LIMITER



BL9C - 3

SINGLE SLOT

f_o = 9.49 GHz

Li @ f_o = 0.8 dB

BANDWIDTH (3dB) = 0.650 GHz

FIGURE 20 LOW LEVEL RF PERFORMANCE OF SINGLE SLOT BULK LIMITER

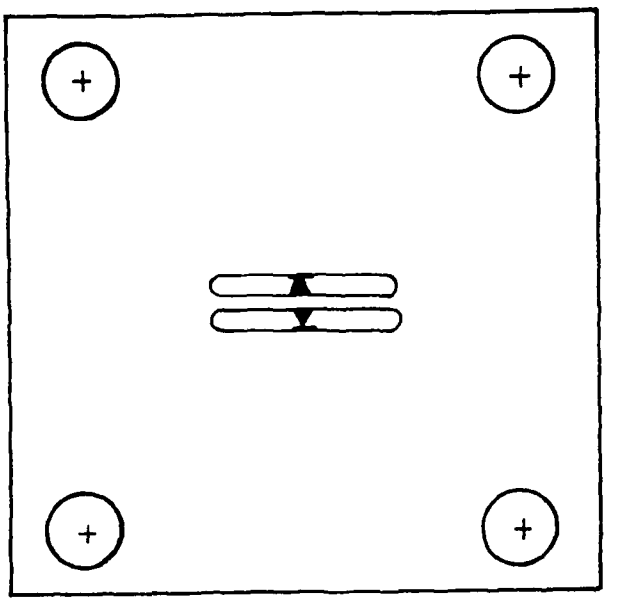
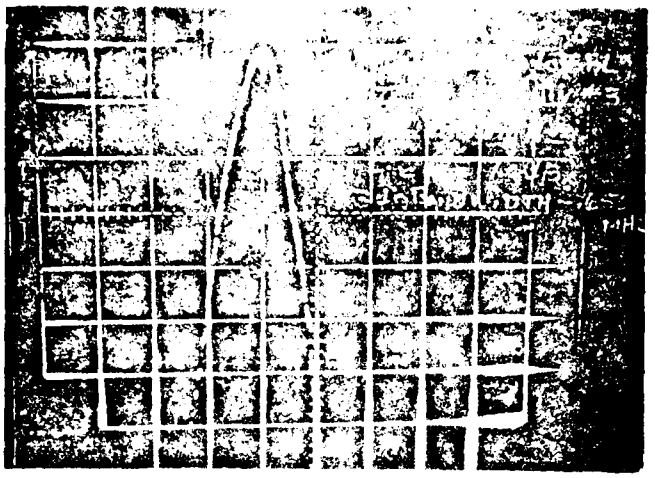


FIGURE 21 DUAL SLOT BULK LIMITER



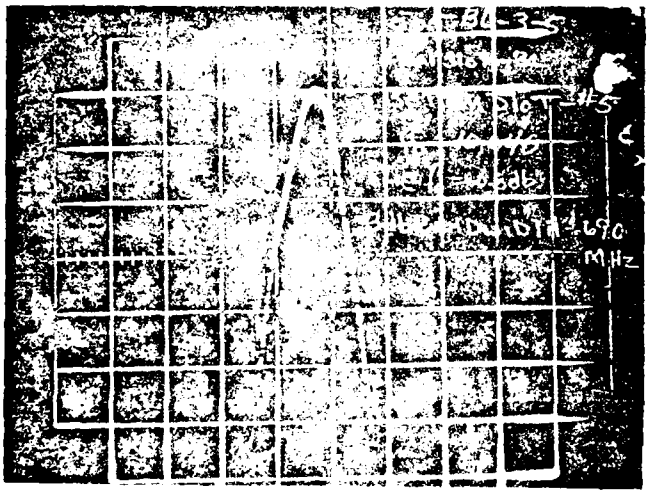
535 BL-3-5

TOP SLOT #3

(a) f_o = 9.8 GHz

Li @ f_o = 1.0 dB

BANDWIDTH (3dB) = 0.650 GHz

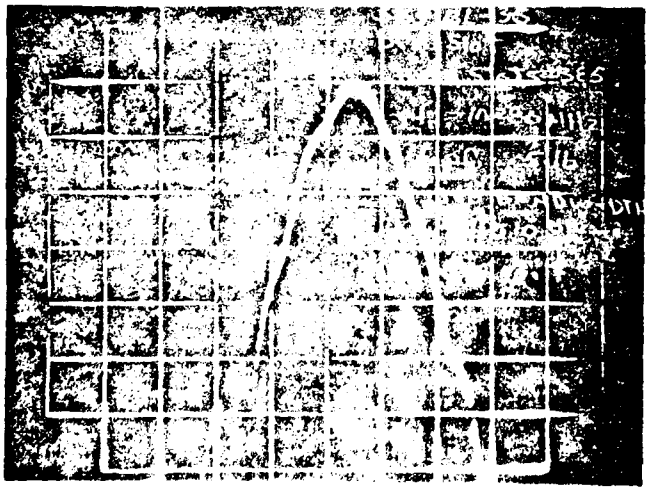


BOTTOM SLOT #5

(b) f_o = 10.04 GHz

Li @ f_o = 0.8 dB

BANDWIDTH (3dB) = 0.690 GHz



DUAL SLOT -- 3 & 5

(c) f_o = 10.280 GHz

Li @ f_o = 0.5 dB

BANDWIDTH (3dB) = 10.01 GHz

PERFORMANCE OF DUAL SLOT BULK LIMITER

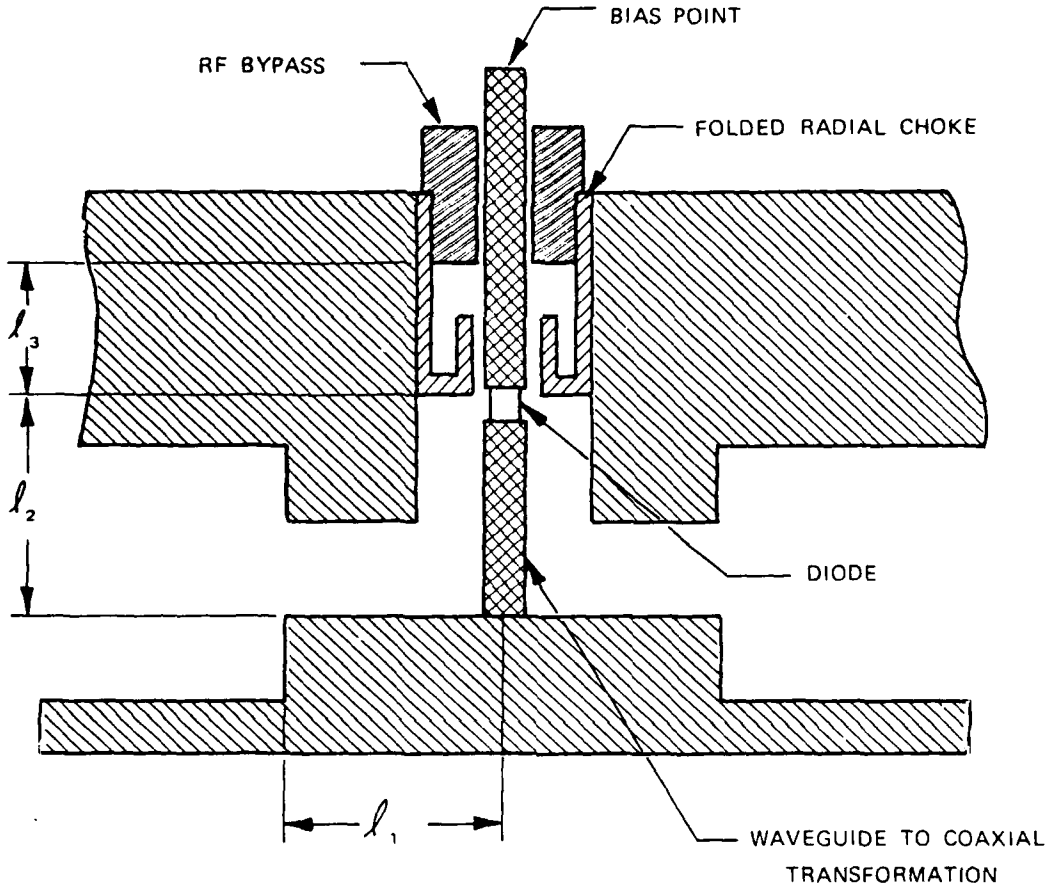


FIGURE 23 DIODE LIMITER CROSSECTION

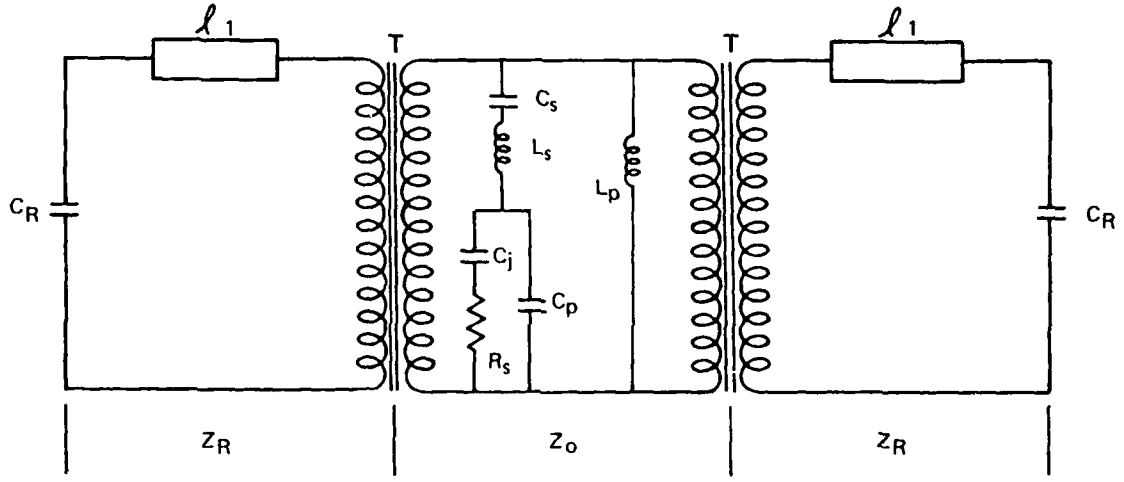


FIGURE 24 EQUIVALENT CIRCUIT OF A DIODE MOUNT

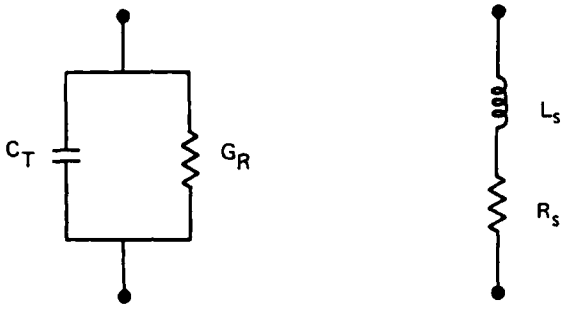


FIGURE 25 SIMPLIFIED DIODE EQUIVALENT CIRCUITS

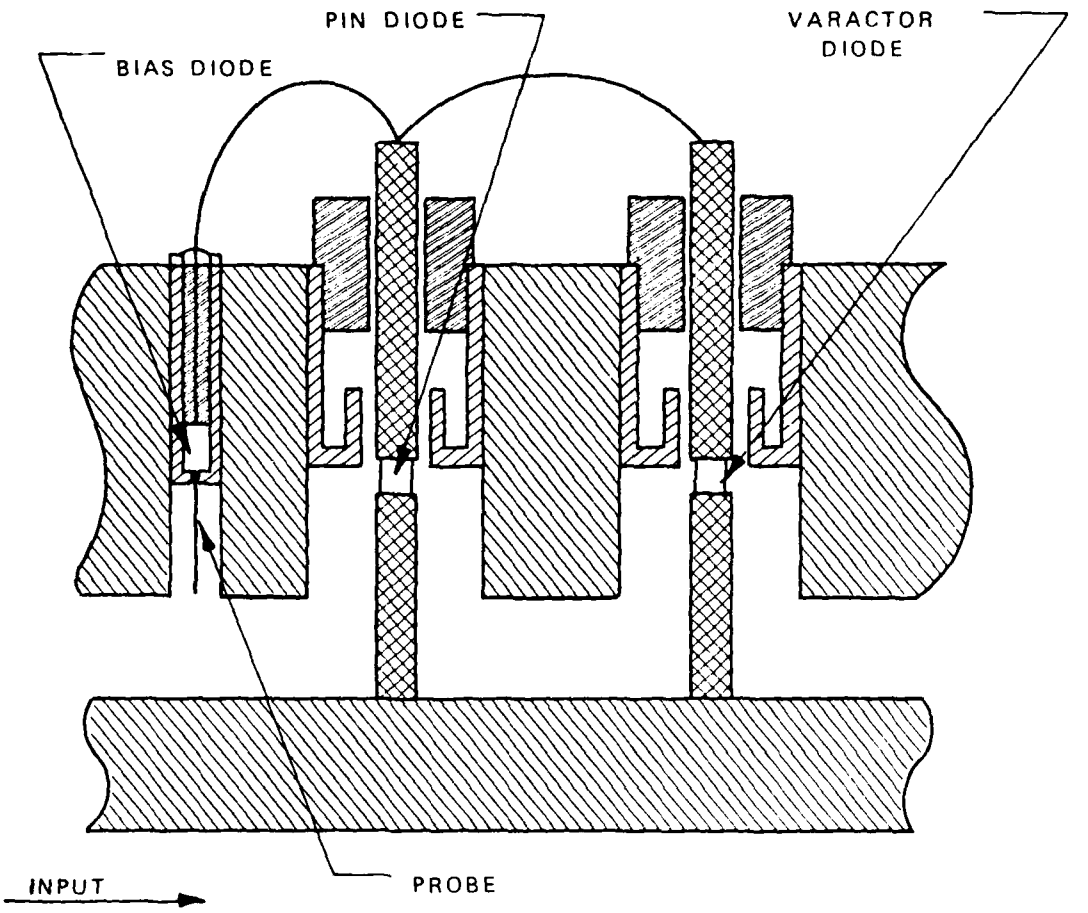


FIGURE 26 CLEANUP LIMITER CROSSECTION

D 15308

The input stage is a high power PIN diode which does the main limiting job. The output stage is a low power varactor used for additional clean-up isolation. A detector diode is used to provide DC bias to the limiter diodes.

Figure 27 shows a schematic of the biasing arrangement. The resistor is used to provide the diodes with a discharge path to ground. This is necessary to shorten the recovery time. This type of limiter design is a highly reliable one. It will withstand environmental extremes of temperature, shock, vibration, humidity, etc., without degradation. Its insertion loss is only 0.4 dB, while it provides a mimimum of 40 dB isolation across the band.

1. Bulk-Diode Limiter Package

The bulk-diode limiter package which comprises the first engineering samples is shown in Figure 28. In combining the bulk limiter with the diode limiter, it was necessary to use tuning screws to achieve optimal broadband performance. The bulk limiter is a very narrow band deivce. The effect of the tuning screws is to transform into and out of the bulk limiter stage. Thus, it becomes better matched across the band.

The relative spacings of the screws, the bulk limiter and the clean-up limiter are also critical. Much time was spent in experimentally determining the spacings which would give optimal broadband performance.

One of the goals of this program is to be able to replace bulk limiters without the need for retuning the package. Some experimentation has been done along these lines. It has been found that, in order to achieve this goal, the bulk limiters must be very consistent and uniform.

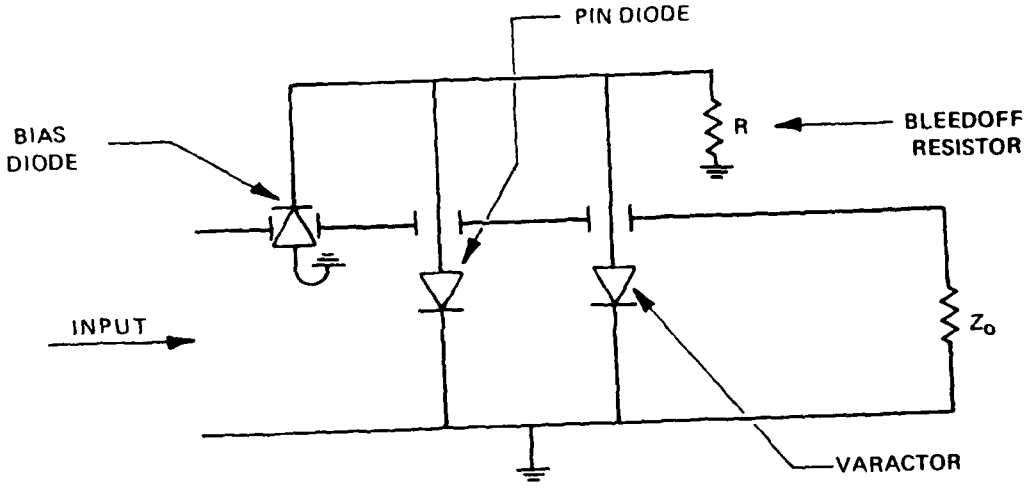


FIGURE 27 CLEANUP LIMITER SCHEMATIC

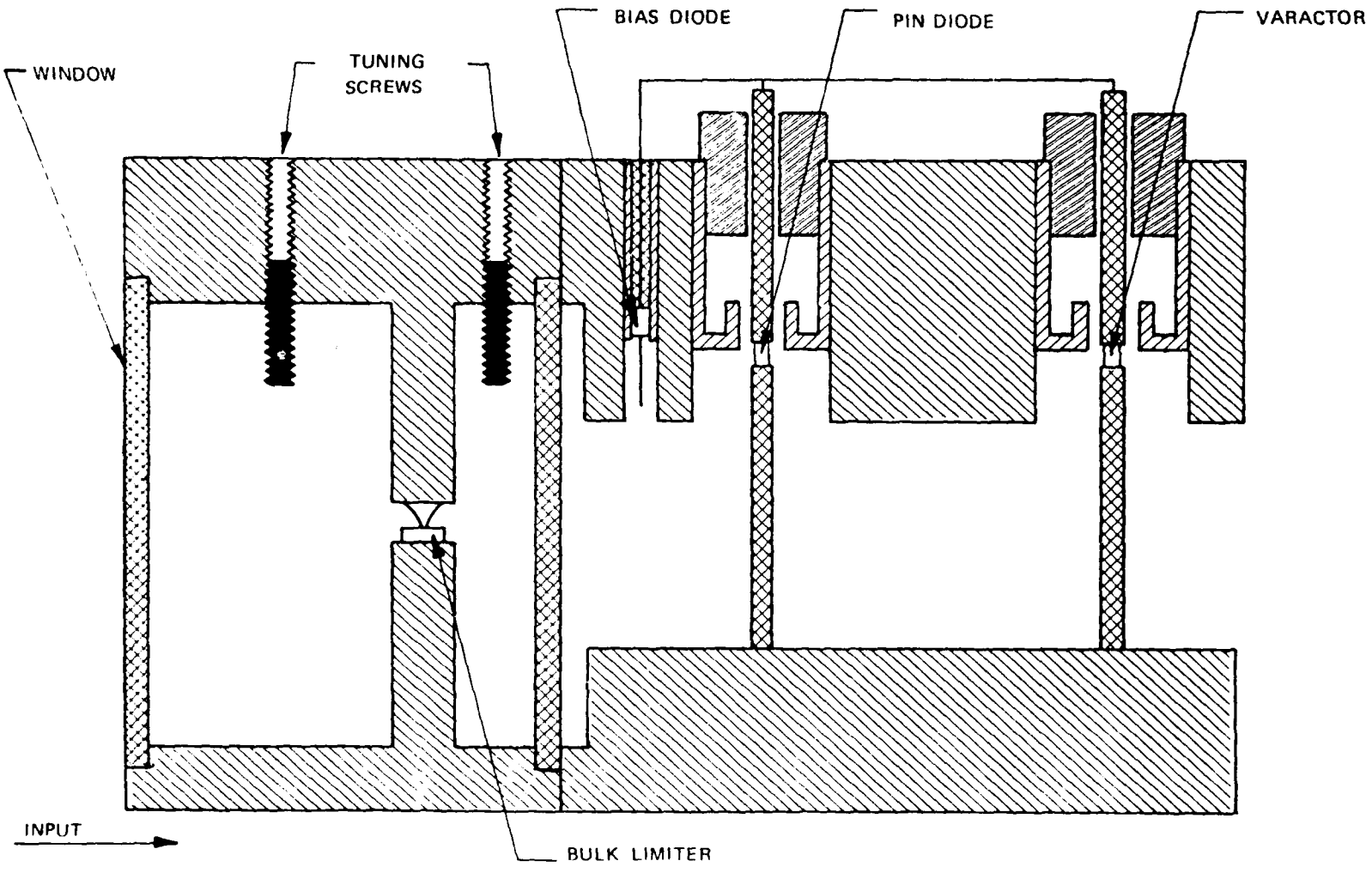


FIGURE 28a BULK DIODE LIMITER

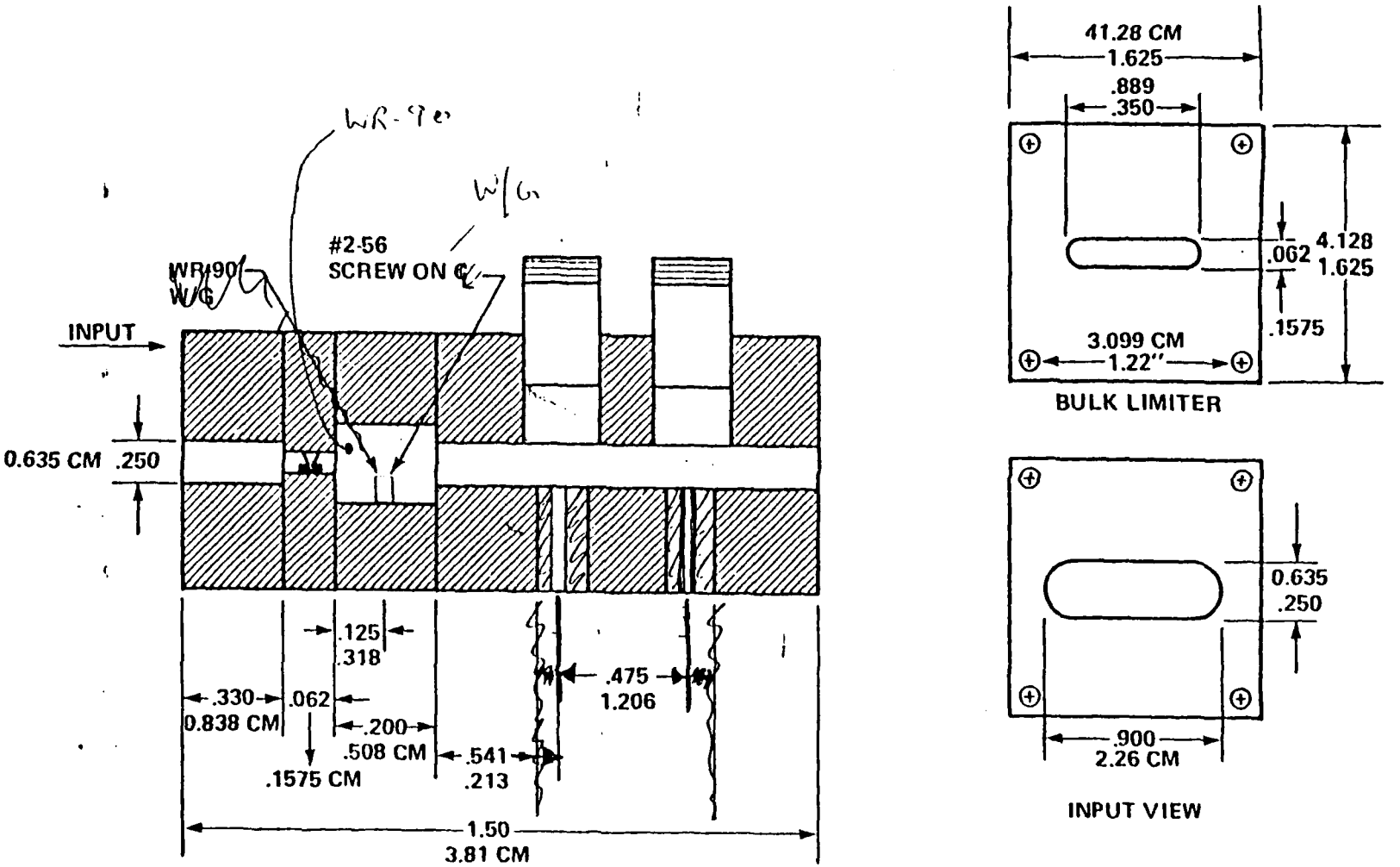


FIGURE 28 (b) BULK-DIODE LIMITER ASSEMBLY

D 19497

The technique used to obtain replaceable bulk limiters to to tune each bulk limiter in a standard, fixed package. Unfortunately, once the bulk limiter has been constructed, the only tuneable parameter is its center frequency. Thus, care must be taken in the manufacture of the bulk limiters to ensure a consistent and uniform quality in such untuneable parameters as insertion loss and bandwidth.

H. Microwave Measurement Facilities and Test Results

1. Low Power Test Facility

The low power microwave test is shown in Figure 29. It consists mainly of an X-band Alfred sweep oscillator (Model No. 8000/7051) and an Alfred network analyzer (Model No. 650). This test set up is used to tune the device for center frequency, low VSWR and insertion loss (see Figure 29).

The sweep oscillator generated an output which covers the 9.0 - 9.65 GHz band. It also provides a horizontal sweep for the network analyzer. The precision attenuator is set so that the power incident upon the device under test is generally below 1 mW.

The two 10 dB directional couplers measure the incident and reflected power of the device under test. The network analyzer compares these two signals to measure return loss. Then VSWR is calculated from the return loss measurement.

The 10 dB coupler behind the device under test samples the power transmitted through it. The network analyzer then compares this signal with the incident power to measure insertion loss.

2. High Power Test Facility

The high power test facility is shown in Figure 30. It consists of a high power X-band magnetron, Model No. 2J51 and a

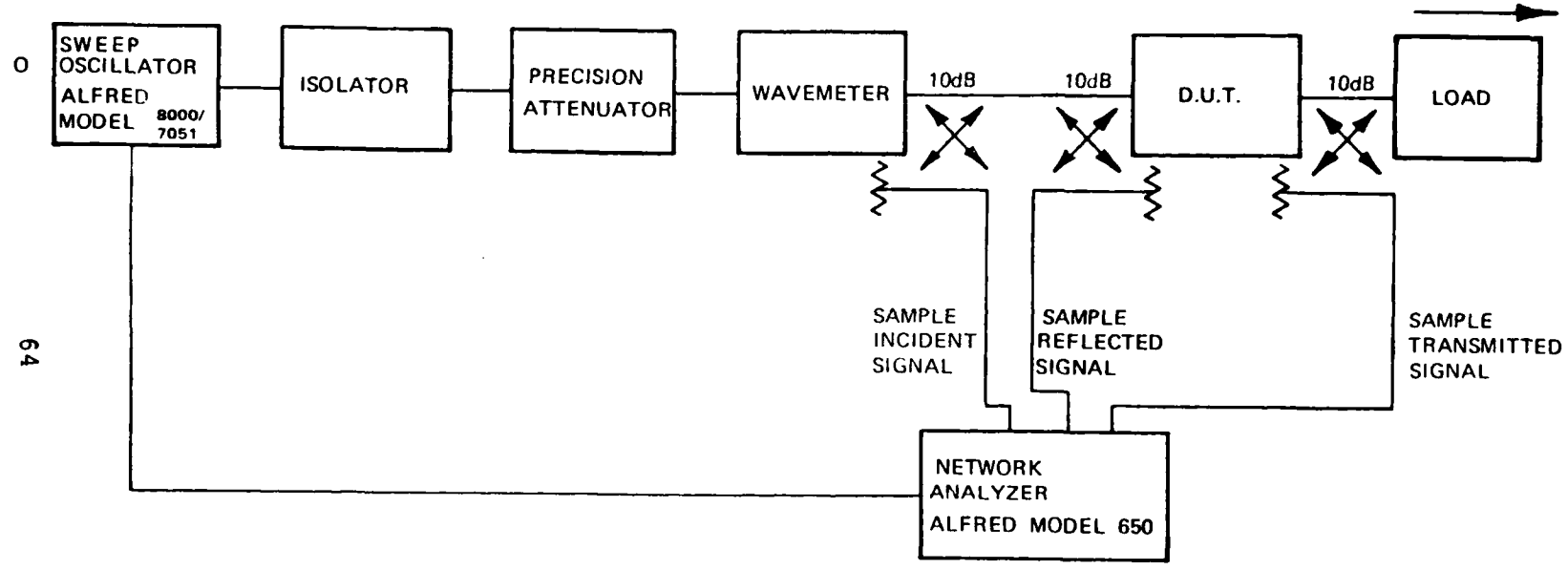


FIGURE 29 LOW LEVEL MICROWAVE TEST FACILITY

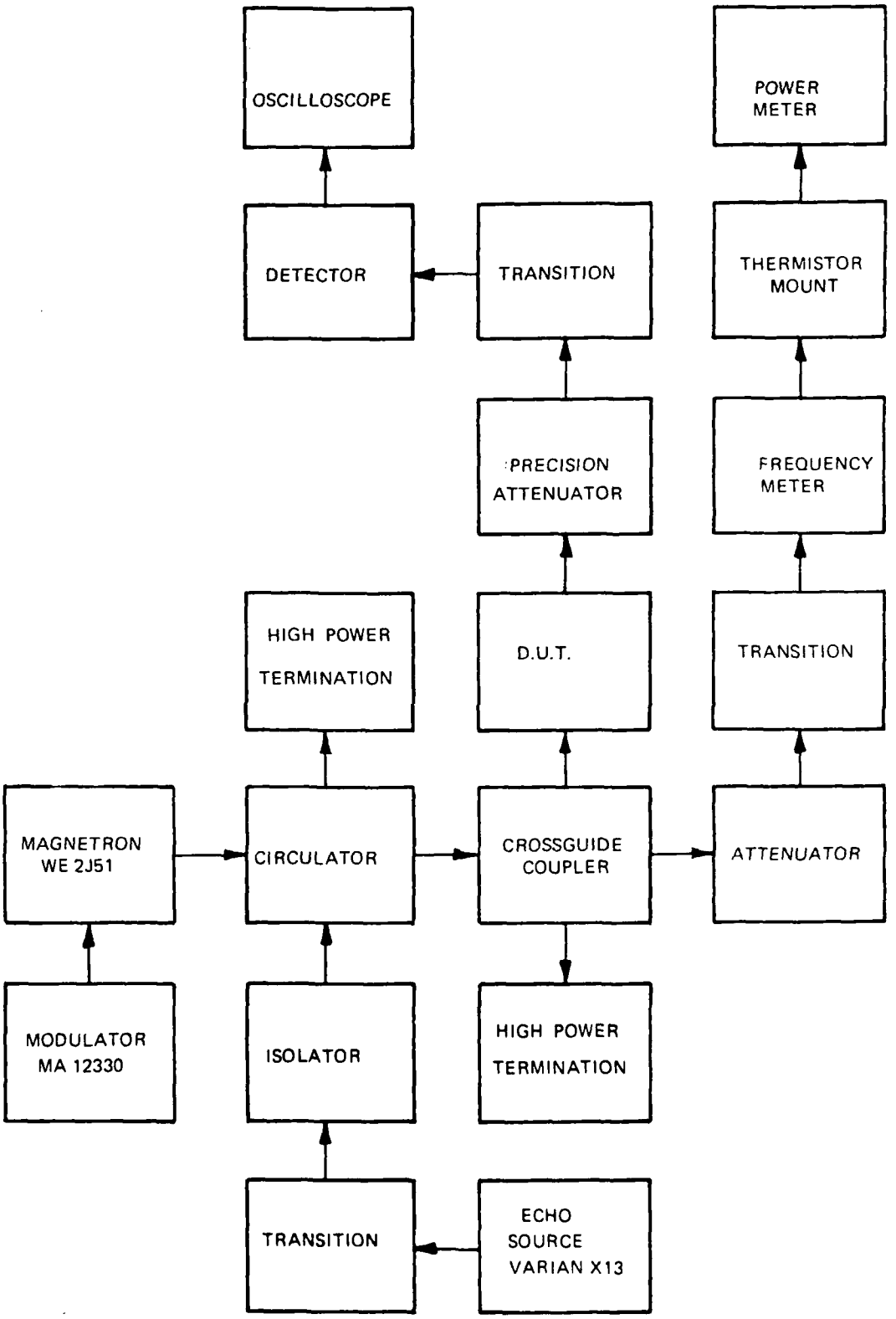


FIGURE 30 MICROWAVE HIGH POWER TEST FACILITY

D-15320

modulator (Model No. MA12330); this system is capable of generating 40 kW with 0.001 duty cycle. The magnetron generates the microwave power, while the modulator controls the pulse and duty cycle conditions.

The circulator serves two functions. First, it protects the magnetron from the power reflected by the device under test. Second, it provides a way of injecting the echo source (Varian Klystron Model No. X-13) signal into the main line. The echo signal permits recovery time measurements to be made. The echo signal enters the circulator and is reflected from the magnetron out to the device under test.

The amount of power in the main RF line is sampled by means of the crossguide coupler. The power meter measures average power. The peak power in the main line is calculated by dividing the average power by the duty cycle. The frequency meter is used to measure the RF frequency in the main line.

3. Flat and Spike Leakage Measurement

Following the device under test are a precision attenuator and a detector. The detector is calibrated so as to give an arbitrary deflection on the oscilloscope for a 10 mW input. The spike and flat leakage through the device under test are determined by adjusting the precision attenuator such that the oscilloscope presentation is returned to the previously determined reference level. The amount of leakage power being measured is then equal to the precision attenuator setting (dB) above 10 mW.

4. Recovery Time Measurement

Recovery time is defined as the time between the end of the RF pulse and the point at which the device under test has

returned to within 3 dB of its insertion loss state. For this measurement, echo signal is introduced along with the magnetron power. The oscilloscope presentation for the recovery measurement is shown in Figure 31. The precision attenuator is varied so as to determine a point which is 3 dB below the steady-state level of the echo signal. The recovery time is measured using the calibrated oscilloscope.

I. Engineering Samples

1. Approval Tests

Successful engineering samples were fabricated and sent to the ERADCOM, Fort Monmouth, NJ for their evaluation. Electrical test results on various engineering sample diodes are given in Table I to Table VI.

2. Preproduction Units and Design Improvements

During this phase of the program, work was concentrated to make bulk limiters reproducible and with high yield. Experiments were also conducted to reduce the insertion loss and to improve the power handling capability of the bulk limiters.[9]

X-band stamped irises (commercially from 0.062 inch thick, oxygen-free, high conductivity copper) were introduced to reduce the price from a $15 machined iris to 20 cents (stamped iris).[10] The confirmatory units results are given in Table VII.

3. Discussion of the Pilot Production Run

Low cost stamped irises and "batch processing" for bulk limiter chips were introduced to manufacture bulk limiters at a low cost. Forty (40) pilot production bulk limiter assemblies consisting of forty bulk limiters and forty clean up limiters were assembled and test results are given in Table VIII.

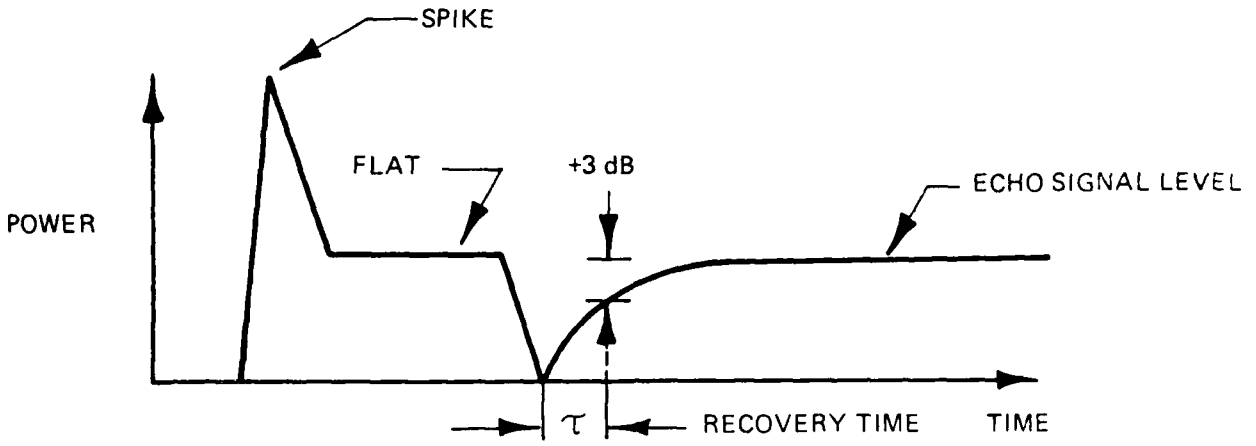


FIGURE 31 RECOVERY TIME MEASUREMENT

OPERATION	PRODUCTION EQUIPMENT	RATE UNITS PER 8 HOURS	YIELD	FINISHED OUTPUT (100 Starts)	STATIONS	CONTROLS
1.01 - Slice Silicon Ingot	Dual Micromatic	200 Wafers	95%	95	1	Micrometer - Thickness
1.02 - Polish Wafer	M/A Polisher	100 Wafers	95%	90	1	Standard Wafer
1.03 - Etch Wafer	Fisher Hood	1000 Wafers	95%	81	1	Visual
1.04 - Check Wafer Thkn	Dual Micromatic	1000 Wafers	95%	77	1	Micrometer - Thickness
1.05 - Phosphor Diffusion	M/A Diffusion Furnace	100 Wafers	95%	73	1	4 Point Probe - Resistivity
1.06 - Silane (SiO_2)	CVD Reactor	100 Wafers	95%	69	1	Sloan Thickness Monitor
1.07 - Open Checker-Board Windows	Dark Room	10 Wafers	80%	55	1	Visual
1.08 - Boron Diffusion	M/A Diffusion Furnace	100 Wafers	95%	52	1	4 Point Probe - Resistivity
1.09 - Annealing	M/A Furnace	50 Wafers	100%	52 Wafers	1	---
1.10 - Metallization (Ti-W-Au)	MRC-900	50 Wafers	80%	48 Wafers	1	Visual
1.11 - Electroplate Gold	M/A Electroplating Bath	20 Wafers	95%	46 Wafers	1	DecTak - Thickness
1.12 - Define Contacts	Dark Room	20 Wafers	95%	43 Wafers	1	---
1.13 - Dicing	M/A Diamond Saw	4 Wafers	80%	160,000 Chips	1	---
1.14 - Electrical Check	Curve Tracer/Boonton	1000 Chips	50%	80,000 Chips	1	---
1.15 - Ball Bonding (5 mil Gold Wire)	M/A Ball Bonder	500 Chips	80%	60,000 Chips	1	Visual
1.16 - Epoxy Junction	Oven	---	90%	54,000 Chips	1	Visual
1.17 - Dice Approval	Curve Tracer/Boonton	500 Chips	90%	46,000 Chips	1	Capacitance & I-V
1.18 - Mounting Chip in Iris	Manual Mounting	200 Chips	60%	27,000	1	Visual
1.19 - Low Power Testing of Bulk Limiter	X-Band Line	500 Chips	20%	5,400	1	Electrical
2.0 - Tuning of Bulk Limiter	Manual	500 Chips	80%	4,300	1	Electrical Meets Spec.

TABLE I BULK LIMITER CHIP PROCESSING

OPERATION	PRODUCTION EQUIPMENT	RATE UNITS PER 8 HRS	YIELD	OUTPUT 100 STARTS	STATIONS	CONTROLS
2.01 - Assemble Limiter Bodies	Soldering Iron, Set Screw Wrenches	20	97%	97	1	Visual
2.02 - Assemble BDL Package	Screwdriver	80	97%	94	1	Visual
2.03 - Low Power Tune	Network Analyzer	8	90%	85	1	Electrical Specification
2.04 - High Power Test	High Power Source	16	90%	76	1	Electrical Specification
2.05 - Finish Assembly	Screwdriver *Soldering Iron*	20	100%	76	1	Visual
2.06 - Electrical Inspection	Network Analyzer, High Power Source	80	100%	76	1	Electrical Specification
2.07 - Mechanical Inspection	Various Plugs and Gauges	160	100%	76	1	Mechanical Specification

TABLE II BULK DIODE LIMITER PACKAGE

SILICON MATERIAL	MEASUREMENT
Type	- p-type
Orientation	- (111)
Resistivity	- 8000 - 15000 ohm-cm
Phosphor Diffusion (resistivity)	- 6 - 7 ohm/cm^{-2}
Boron Diffusion (resistivity)	- 20 ohm/cm^{-2}
Checkerboard Diameter	- 0.75 mil
Contact Area Diameter	- 10 mils in diameter
Capacitance on Chip	- 0.15 pF
V_F at 50 mA	- 2 - 3 Volts

TABLE III DC CHARACTERISTICS OF BULK LIMITER CHIPS

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 2

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	Li	VSWR		Po Note 1	Pf	Ps	Pb	ts		Po Note 1	Pf	Ps	Pb	ts
TEST CONDITIONS	9.0GHz 9.65	9.0GHz 9.65		Frequency - 9.0GHz tp = 1μs, Prr = 1 x 10^3 Du = .001						Frequency - 9.3GHz tp = 1.0 μs, Prr = 1 x 10^3 DU = .001				
MIN. LIMITS	—	—		—	—	—	—	—		—	—	—	—	—
MAX. LIMITS	0.7dB	1.4:1		30kw	50mw	.75w	—	—		30kw	50mw	.75w	—	—
PACKAGE:	BULK LIMITER WITH CLEAN-UP LIMITER													
S/N 1-30R	1.1	1.46		15kw	50mw	1.6w	25mw	8ns		8kw	20mw	1.0w	31mw	5ns
S/N														
S/N 1-6	.9	1.48		9kw	60mw	1.6w	60mw	8ns		7kw	<10mw	1.0w	30mw	6ns
S/N														
S/N 1-10-7	1.0	1.35		10kw	50mw	1.6w	50mw	8ns		8kw	<10mw	5w	31mw	5ns
S/N														
S/N														
S/N 1-BL-3-2	.9	1.58		MICROWAVE ASSOCIATES SEMICONDUCTOR MATERIAL										
S/N 1-BL-3-3	1.1	1.7		MICROWAVE ASSOCIATES SEMICONDUCTOR MATERIAL										
S/N														
S/N				NOTE 1. IN ALL CASES Po WAS DETERMINED WHEN THE RECOVERY TIME REACHED										
S/N				2.0 μsec AT THE 3.0 dB POINT.										
S/N														
S/N														
S/N				TABLE IV(5) LOW AND HIGH POWER TEST RESULTS OF										
S/N				FIRST ENGINEERING SAMPLES WITH CLEAN UP LIMITER										

TESTED BY DATE Q.C. APPROVED BY DATE

FORM 207C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 2

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	Po Note 1	Pf	Ps	Pb	ts
TEST CONDITIONS	Frequency - 9.6GHz tp = 1.0 μs Prr = 1 x 10^3 Du = .001				
MIN. LIMITS	—	—	—	—	—
MAX. LIMITS	30kw	50mw	.75w	—	—
PACKAGE:	BULK LIMITER WITH CLEAN-UP LIMITER				
S/N 1-30R	10kw	<10mw	.5w	20mw	5ns
S/N					
S/N 1-6	10kw	<10mw	.5w	16mw	5ns
S/N					
S/N 1-10-7	9kw	<10mw	.5w	16mw	5ns
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					

NOTE 1. IN ALL CASES Po WAS DETERMINED WHEN THE RECOVERY TIME REACHED 2.0 μsec AT THE 3.0 dB POINT

TABLE IV (b) LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITH CLEAN UP LIMITER

TESTED BY _____ Q.C. APPROVED BY _____ DATE: _____

FORM 7071

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 2

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	Li		f_o		B.W. @3 dB			P_o (1)	P_f	P_s	P_b	t_s		
TEST CONDITIONS	f_o							Frequency -9.0 GHz, t_p = 1 μsec, Prr = 1 X 10^3 Hz, Du = .001						
MIN. LIMITS	---		---		---			---	---	---	---	---		
MAX. LIMITS	---		---		---			---	---	---	---	---		
BULK LIMITER ALONE														
S/N 30R	1.4dB		9.20GHz		.670 GHz			15kW	40 W	100W	40 W	20ms		
S/N														
S/N 6	.8dB		9.16 GHz		.850 GHz			13kW	40 W	160 W	60W	20 ms		
S/N														
S/N 10-7	1.8 dB		9.15 GHz		.930 GHz			15kW	40 W	130 W	60 W	20 ms		
S/N														
S/N														
S/N BL-3-2	1.0		9.30 GHz		1.010 GHz									
S/N BL-3-3	1.6		9.10 GHz		.770 GHz									
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														

NOTE: (1) IN ALL CASES P_o WAS DETERMINED WHEN THE RECOVERY TIME REACHED 2.0 μsec AT THE 3 dB POINT.

TABLE V(a) LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITHOUT CLEAN UP LIMITER

TESTED BY _____ Q.C. APPROVED BY _____ DATE _____

FORM 307C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS -	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2 OF 2	

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	(1) P_o	P_f	P_s	P_b	t_s		(1) P_o	P_f	P_s	P_b	t_s			
TEST CONDITIONS	FREQUENCY - 9.3 GHz t_p = 1.0 μsec, Prr = 1 X 10^3 Hz Du = .001						FREQUENCY - 9.6 GHz t_p = 1 μsec, Prr = 1 X 10^3 Hz Du = .001							
MIN. LIMITS	---	---	---	---	---		---	---	---	---	---			
MAX. LIMITS	---	---	---	---	---		---	---	---	---	---			
BULK LIMITER ALONE														
S/N 30R	20 kW	16 W	100W	16 W	10 ms		15 kW	25W	100W	50W	20 ms			
S/N														
S/N 6	17kW	40W	100W	40W	20 ms		15 kW	20W	130 W	31 W	20 ms			
S/N														
S/N 10-7	15kW	25 W	100W	25 W	20 ms		15 kW	25 W	100 W	40 W	20 ms			
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														
S/N														

NOTE: (1) IN ALL CASES P_o WAS DETERMINED WHEN THE RECOVERY TIME REACHED 2.0 μsec AT THE 3.0 dB POINT

TABLE V (b) LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITHOUT CLEAN UP LIMITER

TESTED BY _____ DATE _____ Q. C. APPROVED BY _____ DATE _____

FORM 1074

PROD. APPROVED	DATE	[redacted]	DS- 3940II	ISSUE
Q.C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 3

SPECIFICATION SCD-A06 LOT SIZE SALES ORDER NO.

PARAMETERS		f_o		L_A f_o		3dB Band-width										
TEST CONDITIONS																
[illegible]		--		--		--										
[illegible]		--		-		--										
	SINGLE SLOT BULK LIMITER WITH CONTINUOUS CLEAN-UP LIMITER															
[illegible]		9400		2.0		.600										
[illegible]		9410		0.4		.700										
[illegible] 5187A-1-7		9410		1.0		.400 [This limiter withstood 40kW when tuned in a package with the clean-up limiter at 9300 + 50 MHz]										
	DUAL SLOT BULK LIMITER WITHOUT CLEAN-UP LIMITER															
[illegible] 1 Top Slot		9000		0.5		.700										
[illegible] Bottom Slot		9010		0.7		.900										
[illegible] Both Slots		9300		0.4		1.750										
[illegible]																
[illegible] 2 Top Slot		9370		0.9		.800										
[illegible] Bottom Slot		9370		0.9		.800										
[illegible] Both Slots		9370		0.6		1.600										

TABLE VI (a) TEST DATA -- DUAL AND SINGLE SLOT BULK LIMITERS WITHOUT ANY CLEAN-UP LIMITER

[illegible] DATE

MOD. APPROVED	DATE	[redacted]	DS - 3940M	ISSUE
D. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS		P_o	P_f	P_t			P_o	P_f	P_t			P_o	P_f	P_t	
TEST CONDITIONS		tp=1.0μsec; Prr=1x10³Hz Du.=.00[illegible] Frequency-[illegible]Hz					tp=1.0μsec; Prr=1x10³Hz Du.=.001 Frequency-9.[illegible]Hz					tp=1.0μsec; Prr=1x10³Hz Du.=.00[illegible] Frequency-9.6[illegible]Hz			
[illegible]		--	--	--			--	--	--			--	--	--	
[illegible]		30KW	--	0.8μsec			30KW	--	0.8μsec			30KW	--	0.8μsec	
	STOP [illegible]														
[illegible] B		27.5KW	22w	1.0μs			25KW	25w	1.0μs			20KW	19w	1.5μs	
[illegible]		[illegible]	[illegible]	[illegible]			[illegible]	[illegible]	2.0μs			17.5KW	31w	2.0μs	
[illegible]	[illegible]														
[illegible] 1 Top Slot		10.0KW	40w	1.5μs			10.0KW	100w	1.0μs			3.0KW	31w	2.0μs	
[illegible] Bottom Slot		10.0KW	40w	1.5μs			10.0KW	60w	1.5μs			3.0KW	60w	2.0μs	
[illegible] Both Slots		10.0KW	200w	1.2μs			10.0KW	130w	1.2μs			10.0KW	160w	1.9μs	
[illegible]															
[illegible] Top Slot		10.0KW	20w	1.5μs			10.0KW	25w	1.2μs			10.0KW	25w	1.8μs	
[illegible] Bottom Slot		10.0KW	16w	1.2μs			10.0KW	12w	1.2μs			10.0KW	16w	1.4μs	
[illegible] Both Slots		10.0KW	100w	1.2μs			10.0KW	100w	1.2μs			10.0KW	50w	1.2μs	
[illegible]															
[illegible]															
[illegible]															

TABLE VI (a) Cont'd.

[illegible] DATE

P.E. APPROVED	DATE			DWG. 3904030	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET		SHEET 3 OF 3	

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS		Li at 9.0GHz		Li at 9.3GHz		Li at 9.65GHz		VSWR at 9.0GHz		VSWR at 9.3GHz		VSWR at 9.65GHz			
TEST CONDITIONS															
MIN. LIMITS		--		--		--		--		--		--			
MAX. LIMITS		0.7dB		0.7dB		0.7dB		1.4:1		1.4:1		1.4:1			
		DUAL SLOT BULK LIMITERS TUNED IN PHASE WITH CLEAN-UP LIMITER													
S/N															
S/N 1		0.8dB		0.8dB		0.8dB		1.25		1.29		1.10			
S/N															
S/N 1		0.8dB		0.8dB		0.8dB		1.24		1.27		1.20			
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															

TABLE VI (a) Cont'd.

TESTED BY P. [illegible] DATE

FORM 1017C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	fo	Li	3dB Band-width			Li	VSWR	Band-width							
TEST CONDITIONS		@fo				9.0GHz to 9.65	9.0GHz to 9.65								
MIN. LIMITS	--	--	--			--	--	--							
MAX. LIMITS	(GHz)	--	(GHz)			.8dB	1.4:1	(GHz)							
	Bulk	Limiter	Alone												
S/N 17ALE-2	9.300	.4	1.20												
S/N 17ALE-3	9.300	.5	1.22												
S/N 17ALE-4	9.310	.4	1.22												
S/N 16A-13	9.300	.5	1.15												
S/N 17A-34	9.310	.4	1.030												
S/N															
S/N		Bulk	Limiters in Package wi n Clean-up Limiter												
S/N 17ALE-2						1.4	1.47	.640	@ 1.47:1						
S/N 17ALE-3						1.1	1.44	.650	@ 1.44:1						
S/N 17ALE-4						1.3	1.45	.650	@ 1.45:1						
S/N 16A-13						1.4	1.56	.650	@ 1.56:1						
S/N 17A-34						1.6	1.70	.630	@ 1.70:1						
S/N															
S/N															
S/N															
S/N															

TABLE VI (b) TEST DATA -- BULK LIMITERS IN PACKAGE WITH CLEAN-UP LIMITER

TESTED BY: TE: Q C APPROVED BY: DATE:

FORM 707 C

PROD APPROVED	DATE		DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	P_F	P_S	R_T		P_F	P_S	R_T		P_F	P_S	R_T				
TEST CONDITIONS	Du = .001 Tp = 1.0 µs Frequency - 9.0GHz PIN = 5.5 kW				Du = .001 Tp = 1.0 µs Frequency = 9.3GHz PIN = 5.5 kW				Du = .001 Tp = 1.0 µs Frequency - 9.6GHz PIN = 5.5 kW						
MIN. LIMITS	-	-	-		-	-	-		-	-	-				
MAX. LIMITS	(w)	(w)	(µs)		(w)	(w)	(µs)		(w)	(w)	(µs)				
	Bulks Limiters Alone														
S/N 17ALE-2	100	200	2.0		40	200	2.6		50	200	3.0				
S/N 17ALE-3	50	160	2.0		40	200	2.6		50	200	3.0				
S/N 17ALE-4	40	200	1.5		40	200	1.8		45	200	2.0				
S/N 16A-13	40	160	1.4		40	200	1.6		40	200	1.8				
S/N 17A-34	31	100	1.2		31	100	1.2		40	100	1.4				
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															

TABLE VI (b)

TESTED BY: Q.C. APPROVED: DATE:

80

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS- 39040XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 3	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	P_F	P_S	R_T	P_b		P_F	P_S	R_T	R_b		P_F	P_S	R_T	P_b	
TEST CONDITIONS	Du = .001 tp = 1.0 µsec Frequency = 9.0GHz PIN = 5.5 kW					Du = .001 tp = 1.0 µsec Frequency = 9.3 GHz PIN = 5.5 kW					Du = .001 tp = 1.0 µsec Frequency = 9.65 GHZ PIN = 5.5 kW				
MIN. LIMITS	-	-	-	-		-	-	-	-		-	-	-	-	
MAX. LIMITS	50mw	.75w	.8µs	(mw)		50mw	.75w	.8µs	(mw)		.50mw	.75mw	.8µs	(mw)	
	Bulk Limiters in Package with Clean-up Limiter														
S/N 17ALE-2	<10	.250	2.6	20		<10	.250	2.7	18		<10	.250	2.6	15	
S/N 17ALE-3	<10	.250	2.6	18		<10	.250	2.7	16		<10	.250	3.0	<10	
S/N 17ALE-4	<10	.250	1.8	15		<10	.250	2.0	18		<10	.250	2.0	18	
S/N 16A-13	<10	.250	1.6	16		<10	.250	1.6	20		<10	.310	1.8	<10	
S/N 17A-34	<10	.250	1.2	16		<10	.250	1.2	18		<10	.250	1.4	16	
S/N															
S/N															
S/N															
S/N															
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S/N															
S/N															
S/N															

TABLE VI (b)

TESTED BY: Q.C. APPROVED BY: DATE:

FORM 807 C